respectively in a manner similar to that as disclosed with reference to the digital data receivers and searcher receiver of the mobile unit in FIG. 2. However, the processing by the digital data receivers and the searcher receivers are different for the mobile to cell-site link from that used in the cell-site to mobile link in several respects.

In the inbound, or mobile unit to cell-site link, the mobile unit does not transmit a pilot signal that can be used for coherent reference purposes in signal processing at the cell-site. Thus, the mobile unit to cell-site link utilizes a non-coherent modulation and demodulation scheme using 64-ary orthogonal signalling.

Searcher receiver 64 is again used to scan the time domain about the received signal to ensure that the associated digital data receiver 66, and data receiver 68 if used, are tracking and processing the strongest available, i.e. received time domain signal. This tracking process is identical to that described with reference to the mobile unit. Searcher receiver 64 provides a signal to cell-site control processor 78 which provides control signals to digital data receivers 66 and 68 for selecting the appropriate received signal for processing.

In the 64-ary orthogonal signalling process, the mobile unit transmitted symbols has one of 64 different possibilities. A 6 bit symbol is encoded into one of 2^6, i.e. 64, different binary sequences. The set of sequences chosen are known as Walsh functions. The optimum receive function for the Walsh function is the Fast Hadamard Transform (FHT). In searcher receiver 64 and digital data receivers 66 and 68, the input signal is correlated as discussed with reference to the mobile unit receivers, with the correlator output fed to a FHT processor. The FHT processor produces a set of 64 coefficients for every 6 symbols. The 64 symbols are then multiplied by a weighting function generated in the receiver. The weighting function is linked to measured signal strength. The weighted data is then provided as an output to diversity combiner and decoder circuitry 80.

The second receiver system processes the received signals in a manner similar to that discussed with respect to the first receiver system of FIG. 3. The weighted 64 symbols output from receivers 66 and 76 are provided to diversity combiner and decoder circuitry 80. Circuitry 80 includes an adder which adds the weighted 64 symbols from receiver 66 to the weighted 64 symbols from receiver 76. The resulting 64 coefficients are compared with one another in order to determine the largest coefficient. The magnitude of the comparison result, together with the identity of the largest of the 64 coefficients, is used to determine a set of decoder weights and symbols for use within a Viterbi algorithm decoder implemented in circuitry 80.

The Viterbi decoder is preferably of a constraint length 9, and of a code rate ½. The Viterbi decoder is utilized to determine the most likely information bit sequence. For each vocoder data block, nominally 15 msec. of data, a signal quality estimate is obtained and transmitted as a mobile unit power adjustment command along with data to the mobile unit. Further information on the generation of this quality estimate is discussed in further detail in the co-pending application mentioned above. This quality estimate is the average signal-to-noise ratio over the 15 msec. interval.

In FIG. 3 optional digital data receiver 68 may be included for improved performance of the system. This additional data receiver alone or in combination with additional receivers can track and receive other possible delay paths of mobile unit transmitted signals. The structure and operation of this receiver is similar to that described with reference to the digital data receivers 66 and 76. Receiver 68 is utilized to obtain additional diversity modes. Optional additional digital data receivers providing additional diversity modes are extremely useful in those cell-sites which are located in dense urban areas where many possibilities for multipath signals occur.

Signals from the MTSO are coupled to the appropriate transmit modulator via digital link 82 under the control of control processor 78. Transmit modulator 84 spread spectrum modulates, according to a predetermined spreading function as assigned by control processor 78, the data for transmission to the intended recipient mobile unit. The output of transmit modulator 84 is provided to transmit power control circuitry 86 where under the control of control processor 78 the transmission power may be controlled. The output of circuitry 86 is provided to transmit power amplifier circuitry 88.

Circuitry 88 includes a summer for summing the output of transmit modulator 84 with the output of other transmit modulators at the cell-site. Circuitry 88 further includes a summer for summing the pilot signal output from pilot signal generator 90 with the summed transmit modulator output signals. Circuitry 88 also includes a digital to analog converter, frequency upconversion circuitry and an amplifier for respectfully converting a digital signal to an analog signal, converting the IF frequency signals as output from the transmit modulators to an RF frequency and amplifying to the RF signal. The output from circuitry 88 is provided to antenna 92 where it is radiated to mobile units within the cell-site service area.

Cell-site control processor 78 has the responsibility for assignment of digital data receivers and modulators to a particular call. Control processor 78 also monitors the progress of the call, quality of the signals and initiates teardown on loss of signal. The cell-site communicates with the MTSO via link 82 where it is coupled by a standard telephone wire, optical fiber, or microwave link.

FIG. 4 illustrates in block diagram form the equipment utilized in the MTSO. The MTSO typically includes a system controller or control processor 100, digital switch 102, diversity combiner 104, digital vocoder 106 and digital switch 108. Although not illustrated additional diversity combiners and digital vocoders are coupled between digital switches 102 and 108.

When the cell-diversity mode is active, the call is processed by two cell-sites, such that signals will arrive at the MTSO from more than one cell-site with nominally the same information. However, because of fading and interference on the inbound link from the mobile unit to the cell-sites, the signal received at one cell-site may be of better quality than the signal receive at the other cell-site.

Digital switch 102 is used in routing the information stream corresponding to a given mobile unit from one or more cell-sites to diversity combiner 104 or the corresponding diversity combiner as determined by a signal from system control processor 100. When the system is not in the cell-diversity mode, diversity combiner 104 may be either bypassed or fed the same information on each input port.

A multiplicity of serial coupled diversity combiners and vocoders are provided in parallel, nominally, one

for each call to be processed. Diversity combiner **104** compares the signal quality indicators accompanying the information bits from the two or more cell-site signals. Diversity combiner **104** selects the bits corresponding to the highest quality cell-site on a frame-by-frame basis of the information for output to vocoder **106**.

Vocoder **106** converts the format of the digitized voice signal to standard **64** Kbps PCM telephone format, analog, or any other standard format. The resultant signals are transmitted from vocoder **106** to digital switch **108**. Under the control of system control processor **100**, the call is routed to the PSTN.

Voice signals coming from the PSTN intended for the mobile unit, are provided to digital switch **108** to an appropriate digital vocoder such as vocoder **106** under control of system control processor **100**. Vocoder **106** encodes the input digitized voice signals and provides the resulting information bit stream directly to digital switch **102**. Digital switch **102**, under the control of system control processor **100** directs the encoded data to the cell-site or cell-sites to which the mobile unit is communicating. If the mobile unit is in a handoff mode communicating to multiple cell-sites or in a cell diversity mode, digital switch **102** routes the call to the appropriate cell-sites for transmission by the appropriate cell-site transmitter to the intended recipient mobile unit. However, if the mobile unit is communicating with only a single cell-site or not in a cell diversity mode, the signal is directed only to a single cell-site.

System control processor **100** provides control over digital switches **102** and **106** for routing data to and from the MTSO. System control processor **100** also determines the assignment of calls to the cell-sites and to the vocoders at the MTSO. Furthermore, system control processor **100** communicates with each cell-site control processor about the assignment of particular calls between the MTSO and cell-site, and the assignment of PN codes for the calls. It should be further understood that as illustrated in FIG. **4** digital switches **102** and **106** are illustrated as two separate switches, however, this function may be performed by a single physical switching unit.

When the cell-diversity mode is in use, the mobile unit will use the searcher receiver to find and trap the strongest multipath signal from each of the two cell-sites. The digital data receivers will be controlled by the searcher receiver and the control processor so as to demodulate the strongest signals. When the number of receivers is less than the number of cell-sites transmitting information in parallel, a switching diversity capability is possible. For example, with only a single data receiver and with two cell-sites transmitting, the searcher will monitor the pilots from both cell-sites and choose the strongest signal for the receiver to demodulate. In this embodiment the choice can be made as frequently as every vocoder frame, or about every 15 milliseconds.

The previous description of the preferred embodiments are provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiment herein, but is to be accorded the widest scope consistent with the principles as novel features disclosed herein.

We claim:

1. A spread spectrum diversity receiver, comprising:

searcher means for, receiving multiple pilot signals each travelling upon a different propagation path and having a resultant time difference with respect to one another, determining signal strength of each received pilot signal and corresponding time relationship with respect to one another, and providing a searcher control signal indicative of received pilot signals of greatest signal strength and corresponding time relationship; and

data receiver means for receiving spread spectrum modulated information signals each corresponding to a different one of said pilot signals, said data receiver means responsive to said searcher control signal for demodulating one of said spread spectrum modulated information signals corresponding to one of said pilot signals of greatest signal strength and for providing an output signal bearing information.

2. The diversity receiver of claim **1** wherein said data receiver means is further responsive to said searcher control signal for demodulating at least one additional one of said spread spectrum modulated information signals each corresponding to a respective other one of said pilot signals of next to greatest signal strength, and providing corresponding additional output signals each bearing said information.

3. The diversity receiver of claim **2** further comprising combiner means for receiving and coherently combining said output signal and said additional output signals and for providing a corresponding combined output signal bearing said information.

4. The diversity receiver of claim **2** further comprising combiner means for receiving and combining said output signal and each of said additional output signal and providing a resultant combined output signal.

5. The diversity receiver of claim **4** wherein said combined output signal bears said information in an error correction coded format and further comprises decoder means for receiving and error correction decoding said combined output signal.

6. The diversity receiver of claim **1** wherein each one of said multiple pilot signals results form a single cell-site transmitted pilot signal travelling different propagation paths to reception by said searcher means, each one of said multiple pilot signals is of a same spreading code offset in time corresponding to its propagation path.

7. The diversity receiver of claim **1** wherein said multiple pilot signals result form different cell-sites each transmitting a single pilot signal spread spectrum modulated by a same spreading code with each cell-site transmitted single pilot signal travelling different propagation paths to reception by said searcher means, each cell-site transmitting its respective single pilot signal at a different code phase offset with respect to each other cell-site transmitted single pilot signal, ones of said multiple pilot signals resulting from a same cell-site transmitted single pilot signal being of a same spreading code offset in time corresponding to its propagation path.

8. In a cellular communication system in which user information signals are communicated to an intended recipient user by a cell-site using spread spectrum communication signals, wherein said cell-site transmits a spread spectrum pilot signal of a predetermined code phase, and wherein said cell-site transmitted spread

spectrum communication signals and pilot signal are susceptible to multipath propagation, a recipient user spread spectrum receiver comprising:

searcher means for receiving an input signal which includes multiple path propagations of a pilot signal transmitted by a cell-site wherein each multiple path propagation pilot signal travels a different propagation path and has a corresponding path dependent offset in code phase, for scanning at different code phases so as to detect a presence of at least one of said multiple path propagation pilot signals, for measuring signal strength of each detected multiple path propagation pilot signal, for determining code phase of each detected multiple path propagation pilot signal, and for providing searcher control signals representative of multiple path propagation pilot signals of greatest signal strength and corresponding code phase; and

receiver means for receiving said searcher control signals, for receiving said input signal which further includes multiple path propagations of spread spectrum communication signals transmitted by said cell-site each corresponding to a respective multiple path propagation pilot signal, for, in response to said searcher control signals, spread spectrum processing certain ones of said multiple path propagations of said spread spectrum communication signals corresponding to said multiple path propagation pilot signals of greatest signal strength so as to extract corresponding intended recipient user information signals therefrom, and for providing corresponding output signals representative of said extracted intended recipient user information signals.

9. The receiver of claim 8 wherein said receiver means comprises a plurality of data receiver means each for, receiving a different one of said searcher control signals, receiving in said input signal said multiple path propagation of spread spectrum communication signals, spread spectrum processing a different selected one of said multiple path propagations of said spread spectrum communication signals in response to said searcher control signals at a synchronization provided by a corresponding multiple path propagation pilot signal, and providing a corresponding one of said output signals.

10. The receiver of claim 8 further comprising combiner means for, receiving said output signals, coherently combining said received output signals and providing a corresponding combined output signal.

11. The receiver of claim 8 further comprising input receiver means for, receiver RF signals in a predetermined frequency band, amplifying said RF signals, frequency downconverting said amplified RF signals to an intermediate frequency range so as to produce corresponding IF signals, filtering said IF signals, digitizing said IF signals, wherein said digitized IF signals correspond to multiple path propagation of said pilot signal and corresponding multiple path propagations of said spread spectrum communication signals, and providing said IF signals to said searcher means and said receiver means as said input signal.

12. In a cellular communication system in which user information signals are communicated to an intended recipient user by at least one cell-site using spread spectrum communication signals, wherein each cell-site transmits a spread spectrum pilot signal of a same spreading code and predetermined different code phase, and wherein each cell-site transmitted spread spectrum communication signals and pilot signal are susceptible to multipath propagation, a recipient user spread spectrum receiver comprising:

searcher means for receiving an input signal including multiple path propagations of at least one pilot signal wherein each pilot signal is transmitted by a respective one of a plurality of cell-sites and wherein each multiple path propagation pilot signal travels a different propagation path and has a corresponding path dependent offset in code phase, for scanning at different code phases so as to detect a presence of at least one of said multiple path propagation pilot signals, for measuring signal strength of each detected multiple path propagation pilot signal, for determining code phase of each detected multiple path propagation pilot signal, and for providing searcher control signals representative of multiple path propagation pilot signals of greatest signal strength and corresponding code phase; and

receiver means for receiving said searcher control signals, for receiving said input signal which further includes multiple path propagations of spread spectrum communication signals transmitted by at least one of said plurality of cell-sites wherein each multiple path propagation of said spread spectrum communication signals corresponds to a respective multiple path propagation pilot signal, for, in response to said searcher control signals, spread spectrum processing certain ones of said multiple path propagations of said spread spectrum communication signals corresponding to said multiple path propagation pilot signals of greatest signal strength so as to extract corresponding intended recipient user information signals therefrom, and for providing corresponding output signals representative of said extracted intended recipient user information signals.

13. The receiver of claim 12 wherein said receiver means comprises a plurality of data receiver means each for, receiving a different one of said searcher control signals, receiving in said input signal and multiple path propagations of spread spectrum communication signals, spread spectrum processing a different selected one of said multiple path propagations of said spread spectrum communication signals in response to said searcher control signals at a synchronization provided by a corresponding multiple path propagation pilot signal, and providing a corresponding one of said output signals.

14. The receiver of claim 12 further comprising combiner means for, receiving said output signals, coherently combining said received output signals and providing a corresponding combined output signal.

15. The receiver of claim 12 further comprising input receiver means for, receiving RF signals in a predetermined frequency band, amplifying said RF signals, frequency downconverting said amplified RF signals to an intermediate frequency range so as to produce corresponding IF signals, filtering said IF signals, digitizing said IF signals, wherein said digitized IF signals correspond to multiple path propagations of said pilot signal and corresponding multiple path propagations of said spread spectrum communication signals, and providing said IF signals to said searcher means and said receiver means as said input signal.

16. In a cellular communication system in which user information signals are communicated to an intended

recipient user by at least one cell-site using spread spectrum communication signals, wherein each cell-site transmits a spread spectrum pilot signal of a same spreading code and predetermined different code phase, and wherein each cell-site transmitted spread spectrum communication signals and pilot signal are susceptible to multipath propagation, a method for acquiring and processing intended recipient user spread spectrum communication signals comprising the steps of:

receiving input signals including (a) multiple path propagations of at least one pilot signal wherein each pilot signal is transmitted by a respective one of a plurality of cell-site and wherein each multiple path propagation pilot signal travels a different propagation path and has a corresponding path dependent offset in code phase and (b) multiple path propagations of spread spectrum communication signals transmitted by at least one of said plurality of cell-sites wherein each multiple path propagation of said spread spectrum communication signals corresponds to a respective multiple path propagation pilot signal;

scanning said input signals at different code phases so as to detect a presence of at least one of said multiple path propagation pilot signals;

measuring signal strength of each detected multiple path propagation pilot signal;

determining code phase of each detected multiple path propagation pilot signal;

providing a searcher signal representative of multiple path propagation pilot signals of greatest signal strength and corresponding code phase;

spread spectrum processing, in response to said searcher signal, ones of said multiple path propagations of said spread spectrum communication signals corresponding to said multiple path propagation pilot signals of greatest signal strength so as to extract corresponding intended recipient user information signals therefrom; and

providing corresponding output signals representative of said extracted intended recipient user information signals.

17. The method of claim **16** further comprising the steps of:

combining said output signals; and

providing a corresponding combined output signal.

18. The method of claim **16** further comprising the steps of:

receiving RF signals in a predetermined frequency band;

amplifying said RF signals;

frequency downconverting said amplified RF signals to an intermediate frequency range so as to produce corresponding IF signals;

filtering said IF signals;

digitizing said IF signals; and

providing said IF signals to said searcher means and said receiver means as said input signals.

* * * * *

EXHIBIT E.

US005107225A

United States Patent [19]

Wheatley, III et al.

[11] Patent Number: 5,107,225

[45] Date of Patent: Apr. 21, 1992

[54] HIGH DYNAMIC RANGE CLOSED LOOP AUTOMATIC GAIN CONTROL CIRCUIT

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[73] Assignee: QUALCOMM Incorporated, San Diego, Calif.

[21] Appl. No.: 620,092

[22] Filed: Nov. 30, 1990

[51] Int. Cl.[5] H03G 3/30

[52] U.S. Cl. 330/279; 455/239.1; 330/281

[58] Field of Search 330/277, 279, 281, 284, 330/302; 332/118, 125; 375/98; 455/239, 241, 251

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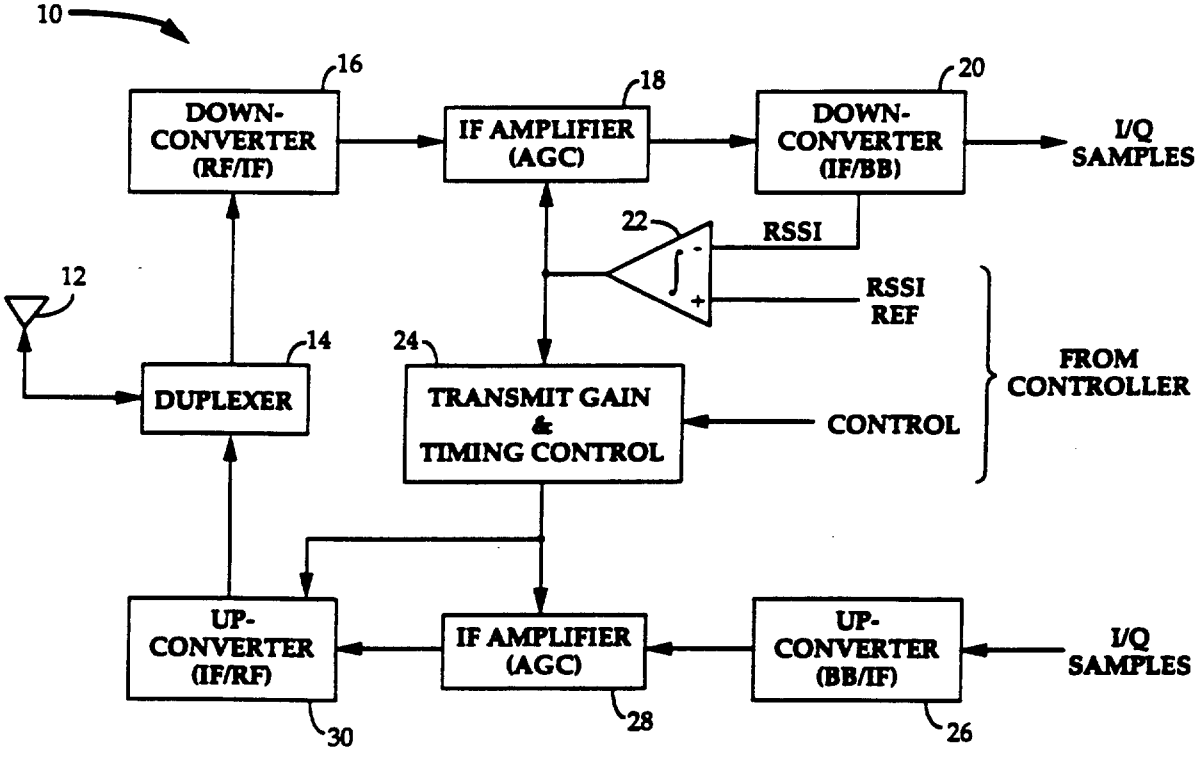
Primary Examiner—Steven Mottola
Attorney, Agent, or Firm—Russell B. Miller

[57] ABSTRACT

A closed loop automatic gain control (AGC) circuit with high dynamic range capabilities having an amplifier circuit for receiving an input signal, which is susceptible to variations in signal power, and a control signal. The amplifier circuit is responsive to the control signal for amplifying the input signal at a gain level corresponding to the control signal so as to provide a corresponding output signal. A measurement circuit is coupled to the amplifier means for measuring logarithmic signal power of the amplified input signal and providing a corresponding linear measurement signal. An integration circuit is included for receiving the measurement signal, and a reference signal which corresponds to a desired signal power of the output signal. The integration circuit integrates with respect to time the difference between the measurement signal and the reference signal, and generates the control signal which corresponds to the result of the integration.

22 Claims, 3 Drawing Sheets



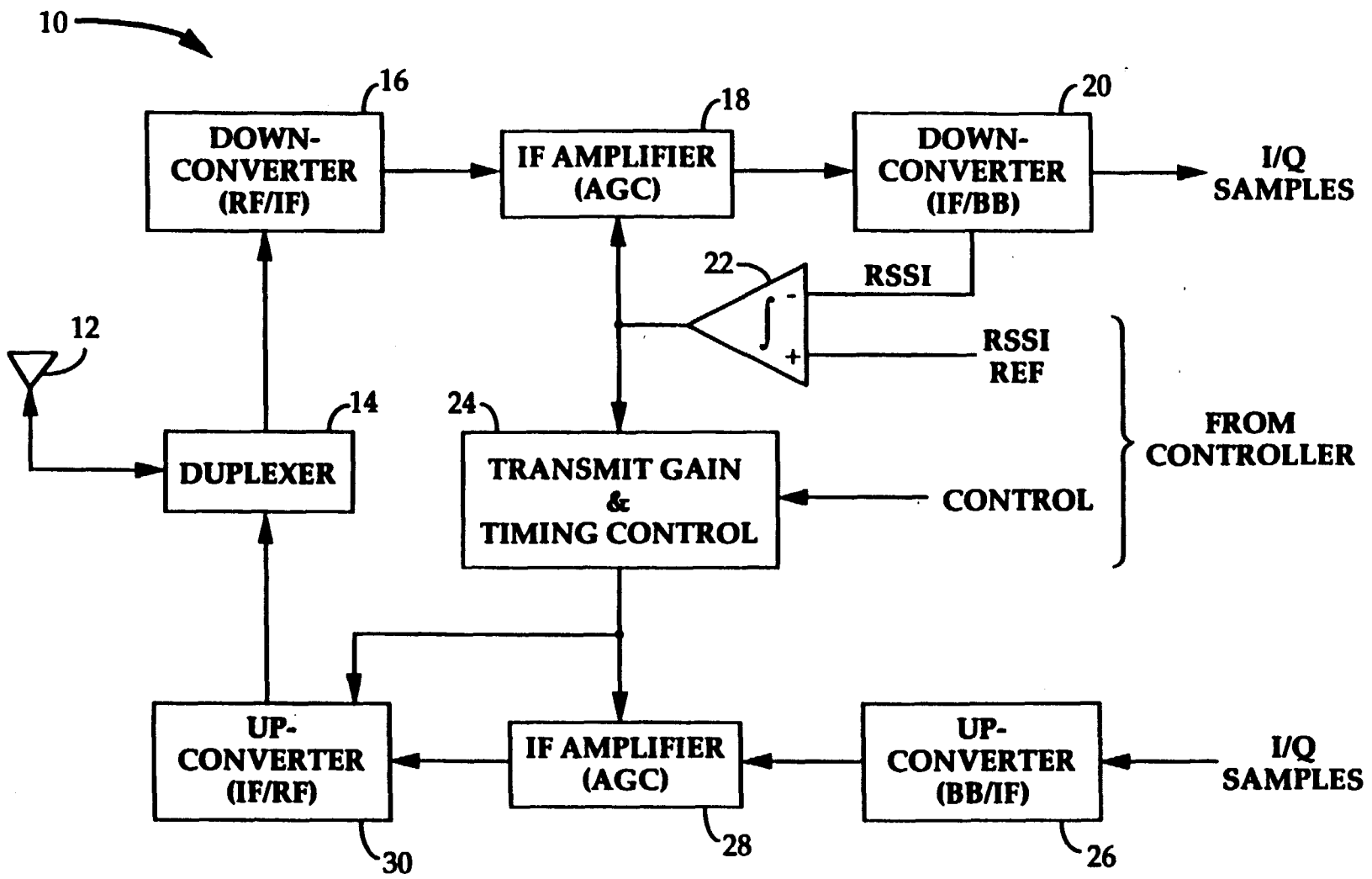

10
16
DOWN-CONVERTER (RF/IF)
18
IF AMPLIFIER (AGC)
20
DOWN-CONVERTER (IF/BB)
I/Q SAMPLES
22
RSSI
RSSI REF
12
14
DUPLEXER
24
TRANSMIT GAIN & TIMING CONTROL
CONTROL
FROM CONTROLLER
UP-CONVERTER (IF/RF)
IF AMPLIFIER (AGC)
UP-CONVERTER (BB/IF)
I/Q SAMPLES
30
28
26

FIG. 1

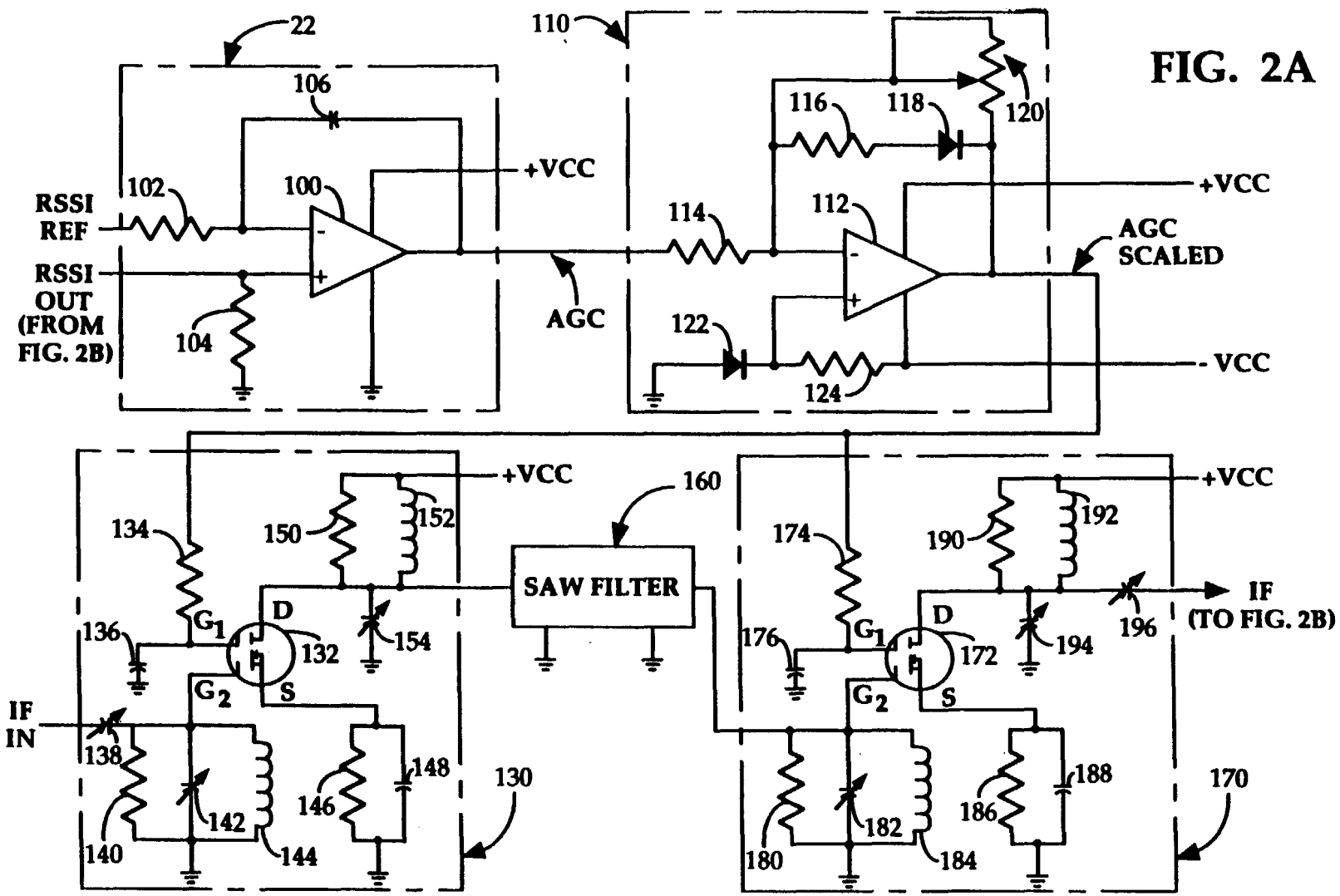

22
110
106
+VCC
RSSI REF
102
100
RSSI OUT (FROM FIG. 2B)
104
AGC
114
116
118
120
112
+VCC
AGC SCALED
122
124
- VCC
+VCC
160
SAW FILTER
134
150
152
G1
D
132
154
136
G2
S
IF IN
138
140
142
144
146
148
130
+VCC
174
190
192
G1
D
172
194
196
IF (TO FIG. 2B)
176
G2
S
180
182
184
186
188
170

FIG. 2A

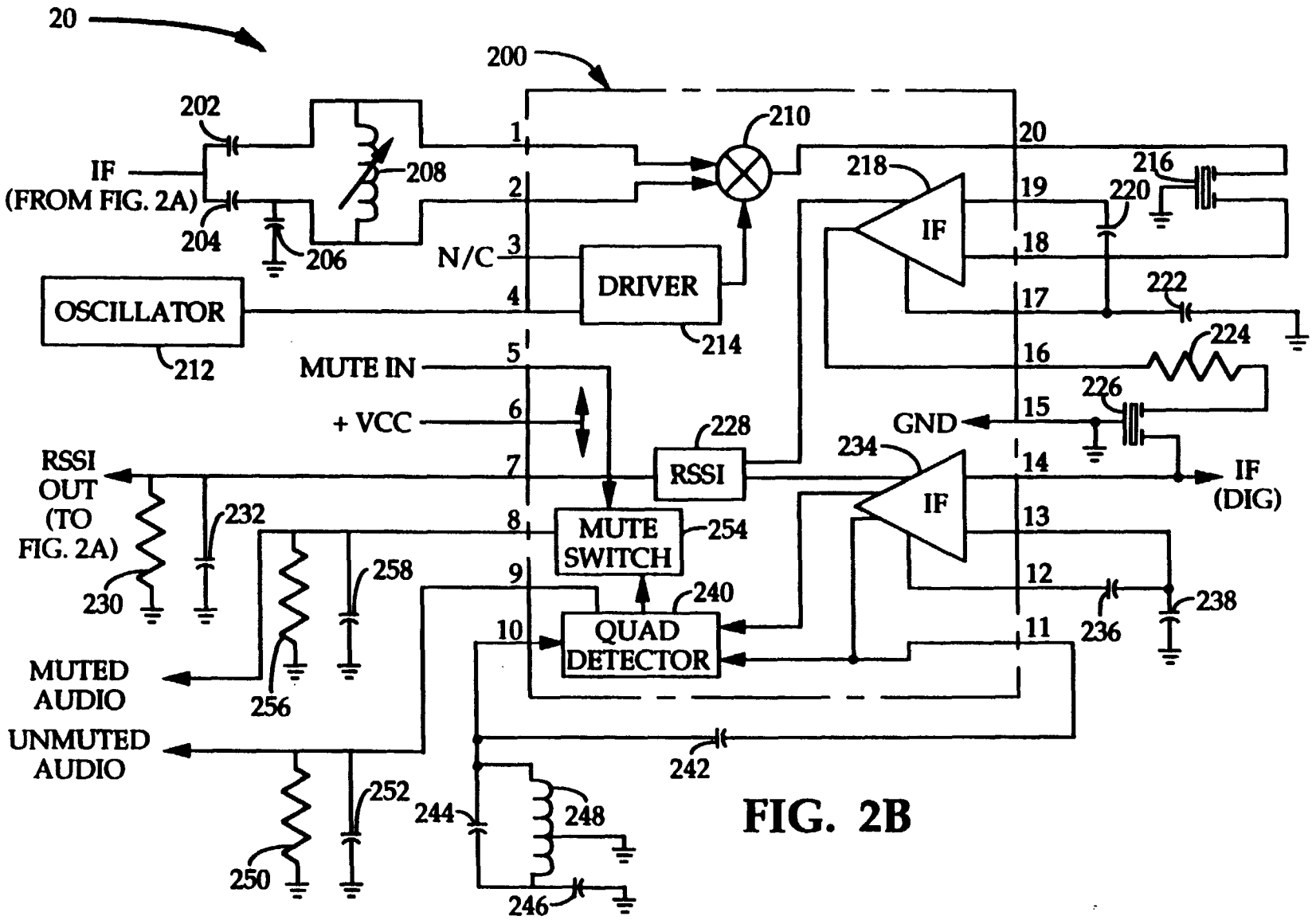

20
200
202
IF
(FROM FIG. 2A)
204
206
208
210
1
2
N/C
3
4
OSCILLATOR
212
DRIVER
214
MUTE IN
5
+ VCC
6
7
RSSI
OUT
(TO
FIG. 2A)
230
232
8
MUTE
SWITCH
254
9
258
240
10
QUAD
DETECTOR
MUTED
AUDIO
256
UNMUTED
AUDIO
250
252
244
248
246
242
218
IF
20
19
18
17
16
15
14
13
12
11
216
220
222
224
226
GND
228
RSSI
234
IF
IF
(DIG)
236
238

FIG. 2B

HIGH DYNAMIC RANGE CLOSED LOOP AUTOMATIC GAIN CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates to automatic gain control circuits. More particularly, the present invention relates to a novel and improved closed loop automatic gain control gain control circuit with linear gain control over a very high dynamic range.

II. Description of the Related Art

Automatic gain control (AGC) circuits are widely used in receivers for controlling the gain applied to a signal to be processed. In both analog and digital signal receivers AGC circuits are implemented using different techniques. In analog receivers analog techniques are commonly used while in digital receivers, digital techniques are applied.

In analog receivers, such as used in narrowband FM cellular telephones, the power of the received signal is merely limited typically by clipping the signal. However, such an analog signal processing technique is not applicable to digital receivers since a clipping of a signal modulated with digital data would result in corruption of the data.

Typically in digital receivers, the level of signal power is detected digitized and then measured. The measured value is typically compared with a set value and an error value generated, all values being in digital form. The error value is then used to control the gain of an amplifier so as to adjust the signal strength to coincide with the desired signal power.

Digital AGC techniques however are relatively slow in controlling signal power due to saturation of the error signals involved in actually controlling the power. Digital techniques thus have the disadvantage of failing to provide accurate power control in environments where signal strength is rapidly changing, and particularly over a high dynamic range.

It is therefore an object of the present invention to provide a novel and improved AGC circuit for rapid, high dynamic range signal power control.

It is yet another object of the present invention to provide an AGC circuit capable of providing gain control over both wideband and narrowband signals so as to maintain received signal power at a constant level.

It is still a further object of the present invention to provide an AGC circuit capable of providing a control signal which can be used in controlling transmitter power.

SUMMARY OF THE INVENTION

The present invention is a novel and improved closed loop automatic gain control circuit which utilizes low cost analog circuitry to measure and control signal power of a received RF signal. In applications where the signal of interest is either a wideband signal, such as a CDMA signal containing digital information, or a narrowband signal, such as an FM signal containing analog information, the circuitry of the present invention is capable of providing the necessary gain control.

In accordance with the present invention a closed loop automatic gain control (AGC) circuit having high dynamic range capabilities is disclosed. THe AGC circuit is comprised of an amplifier means for receiving an input signal which is susceptible to variations in signal power. The amplifier means also receives a control signal and is responsive to the control signal for amplifying the input signal at a gain level in dB as a linear function of a control signal and providing a corresponding output signal. Measurement means is coupled to the amplifier means for measuring logarithmic signal power of the input signal and providing a corresponding linear measurement signal in response to input signal power variations in dB. Integration means is included for receiving th measurement signal, and a reference signal which corresponds to a desired signal power of the output signal. The integration means integrates over time the difference between the measurement signal and the reference signal, and generates the control signal corresponding to the result of the integration.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

FIG. 1 is a block diagram illustrating in an exemplary application the elements of the closed loop automatic gain control circuit of the present invention; and

FIGS. 2A and 2B illustrate in schematical form an exemplary embodiment of the closed loop automatic gain control circuit of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In a digital receiver such as used in a code division multiple access (CDMA) mobile cellular telephone, it is necessary to limit the power of the received signal for proper signal processing of the received signal. In the cellular environment, a digital receiver may receive a signal which experiences rapid and wide variations in signal power. In order to properly process the digital data contained within the received signal the signal power must be limited. Accordingly, a closed loop automatic gain control circuit for a digital receiver is disclosed which is capable of limiting received signal power in such an environment.

FIG. 1 illustrates in block diagram form an exemplary application of the closed loop automatic gain control circuit of the present invention. In FIG. 1, the closed loop automatic gain control circuit is implemented in the transceiver of a CDMA mobile cellular telephone 10. It is envisioned that telephone 10 may be exclusively CDMA compatible or of a dual mode, i.e. CDMA and conventional FM compatible. The closed loop automatic gain control circuit of the present invention is capable of providing power limiting of both wideband CDMA signals and narrowband FM signals. The compatibility of such circuitry to operate on both wideband and narrowband signals provdes cost, component and power savings for the receiver.

Telephone 10 includes antenna 12 for receiving transmitted RF signals, including CDMA or FM communication signals, transmitted from a base station that are intended for reception and processing by mobile telephone 10. Antenna 12 couples the received signals to duplexer 14 which provides the received signals to the receiver portion of telephone 10. Duplexer 14 also receives CDMA or FM communication signals from the transmitter portion of telephone 10 for coupling to antenna 12 for transmission to a base station.

The received signals are output from duplexer 14 to downconverter 16 where the RF signals are converted to a lower frequency range and are provided as corresponding IF signals. The IF signals from downconverter 16 are provided to automatic gain controlled IF amplifier 18. The IF signals are amplified at a gain level determined by an AGC signal also provided to amplifier 18. Amplifier 18 is capable or providing, in response to the AGC signal, linear control of gain in dB over a high dynamic range, such as in excess of 80 dB. Amplifier 18 is preferably of a design described in a copending U.S. Pat. application entitled "LINEAR GAIN CONTROL AMPLIFIER", Ser. No. 07/598,845, filed Oct. 15, 1990, and assigned to the Assignee of the present invention.

The gain controlled IF signals are output from amplifier 18 to a second frequency downconverter, downconverter 20, where the IF signals are converted to a lower frequency range and provided as corresponding user baseband signals. In the embodiment shown in FIG. 1, the baseband signals in the CDMA mode of operation are I and Q samples of encoded digital data which are output for further demodulation and correlation. In a dual mode receiver, downconverter 20 also frequency dowwnconverts and demodulates the FM signals so as to provide an audio signal output.

Downconverter 20 also includes the capability of measuring the strength of the signal received by telephone 10 and generating a corresponding received signal strength indication (RSSI) signal. The RSSI signal along with a RSSI reference signal are provided to integrator 22. The RSSI reference signal is generated by a controller (not shown) and corresponds to a desired signal strength level for the IF signals output from amplifier 18. Integrator 22 generates the AGC signal that is input to amplifier 18 for gain control.

Downconverter 20 enables the use of an analog gain control technique for a digital signal impressed upon a carrier signal, unlike the gain control techniques typically used in digital receivers. In particular, downconverter 20 performs an analog measurement of RF power in the received signal and provides a corresponding RSSI signal. The RSSI signal is a signal which varies linearly with respect to measured log power. This analog power measurement is used to provide control over the power in the received wideband signal so as to maintain the signal, as output for digital signal processing, at a constant power level. Similarly when the received signal is a narrowband signal the power is also maintained at a consant level.

Integrator 22 receives the RSSI signal from downconverter 20 along with the RSSI reference signal. In order to provide accurate power control, is necessary for the error between the RSSI signal (indicative of the measured power level) and the RSSI reference signal (indicative of the desired power level) to be eliminated. Integrator 22 is used to provide this function in the AGC loop by forcing the error to zero. For example, if the gain of the signal is too high, the RSSI signal will also be high as compared to the RSSI reference signal. Until the two input signals to integrator 22 are identical, the integrator output signal will continue to go up resulting in a reduction of the gain of amplifier 18.

It should be understood that the RSSI measurement can be made at various points in the processing of the received signal. Although illustrates in FIG. 1 that the measurement is made in downconverter 20, and at an IF frequency, the measurement can be made in downconverter 16 or at any other point in the signal processing at either an RF or IF frequency.

The use of analog techniques in wideband signal power control provides for a reduction in hardware required for a dual mode telephones. As mentioned previously, in a dual mode telephone wideband and narrowband signal power must be provided for the CDMA signal and the FM signal. In using analog power control techniques for both the wideband and narrowband signals, the same power control circuitry can be used for both modes of operation.

Analog power control techniques provide a faster response to variations in signal power than conventional digital power control techniques. In using analog power control techniques to control a signal power of a wideband signal containing digital data, signal power can be controlled at a faster rate than using conventional digital power control techniques. The exemplary implementation of the AGC loop of the present invention does not limit dynamic errors so as to achieve fast control of gain over a range of 100 dB.

Furthermore, in this embodiment, where a linear control and measurement circuit (linear with respect to voltage vs. dBm) is used, loop bandwidth is independent of signal power. Loop bandwidth is held constant since the gain of each element in the loop is constant over a wide range of signal variations.

With respect to the transmitter portion of telephone 10, transmit power is also controlled. The AGC signal is again used to provide instantaneous control of transmit power. THe AGC signal is provided to the transmitter portion, along with various other control signals from the controller. In utilizing the AGC signal to also control transmit power, the transmitter gain is adjusted with respect to the receiver gain so that the transmitter gain tracks the receiver receiver gain.

In the tranmission of CDMA communication signal from telephone 10 to a base station, the transmitter portion of telephone 10 is provided with user baseband signals, typically I and Q samples of encoded digital data in the single mode telephone. In the dual mode telephone I and Q samples, or FM signals would be provided as the user baseband signals. The I and Q samples, or FM signals, are provided as an input to upconverter 26 where these baseband signals are converted in frequency to a higher frequency range and provided as IF signals. The IF signals are then provided to IF amplifier 28 where amplified at a level determined by the AGC signal provided through logic 24.

The amplified IF signals are provided to upcoverter 30 where they are converted in frequency to a higher frequency range and provided as RF signals. Upconverter 30 also includes an amplifier and receives signals from logic 24 for controlling the gain of the RF signals output therefrom. The RF signals are then provided to duplexer 14 which couples the signals to antenna 12 for transmission.

It is to be noted that the application of the same AGC signal which controls the receiver gain to IF amplifier 28 provides an advantage to the telephone operation. The use of the AGC signal by the transmitter permits the transmitter gain to track receiver gain. For example, as the received signal increases in signal strength, less transmission signal power is needed to maintain communications from the telephone to the base station. Accordingly, with the receiving AGC circuit forcing a decrease in gain for the received signal, the transmission gain is correspondingly decreased.

Turning now to FIGS. 2A and 2B illustrated therein is further details of the exemplary embodiment of the closed loop automatic gain control circuit of FIG. 1 as implemented in the receiver portion of telephone 10. FIGS. 2A and 2B in particular illustrate amplifier 18 downconverter 20 and integrator 22 as main elements of the closed loop.

In FIG. 2A, integrator 22 is comprised of an operational amplifier, op amp 100, having a feedback network to configured to such that op amp 100 functions as an integrator. In particular, op amp 100 receives the RSSI reference signal through resistor 102 at its inverting input. The RSSI out signal (described in further detail below) is input to the noninverting input of op amp 100, while the noninverting input is also coupled to ground through resistor 104. The output of op amp 100 is coupled to the inverting input of op amp 10 through capacitor 104. Integrator 22 produces an output voltage which is proportional to the integral, i.e. the product of the amplitude and duration, of the difference between the RSSI reference signal and the RSSI out signal. The RSSI reference signal being indicative of a desired signal strength while the RSSI out signal is indicative of measured signal strength. The output signal from op amp 100 is an uncompensated AGC signal that is coupled as an input to IF amplifier 18.

IF amplifier 18 is comprised of compensation circuit 110, amplifier circuit 130, filter 160 and amplifier circuit 170. Compensation circuit 110 receives the AGC signal and in response thereto generates a compensation signal, AGC SCALED, which compensates for nonlinearities in gain control over the dynamic range of amplifier circuits 130 and 170. The compensation signal is output from compensation circuit 110 to both amplifier circuits 130 and 170.

Amplifier circuit 130 receives and amplifies an input IF signal at a gain level determined by the AGC SCALED signal. The amplified IF signal is then output to filter 160 where it is bandpass filtered and output to amplifier circuit 170. Amplifier circuit 170 receives the amplified and filtered IF signal where amplified at a gain level determined by the compensation signal. The amplified IF signal is then output from amplifier circuit 170 for further processing.

Compensation circuit 110 is comprised of an operational amplifier, op amp 112, which has an inverting input coupled to receive the AGC signal through input resistor 114. The inverting input is also coupled to the output of op amp 112 through a nonlinear feedback circuit comprised of series coupled resistor 116 and diode 118 which are coupled in parallel with variable resistor 120. The noninverting input of op amp 112 is provided with a reference or bias voltage across diode 122 that is provided through resistor 124 from the supply voltage -VCC. Resistors 114, 116 and 124 are typically of the same resistance, e.g., 10KΩ value, while variable resistor 120 is capable or providing a much larger resistance value, e.g. 50KΩ.

In the operation of compensation circuit 110, when the AGC SCALED signal voltage is below the bias voltage appearing at the noninverting input of op amp 112, the parallel resistance combination of resistor 116 and variable resistor 120, along with input resistor 114 ((R116|R120)/R114) sets a first slope gain curve for operation of op amp 112. When the AGC SCALED signal voltage is above the bias voltage, the value of variable resistor 120 along with input resistor 114 (R120/R114) sets a second, and different, gain curve for operation of op amp 112. Furthermore diodes 118 and 124 are preferably of the same type such that changes in temperature affecting diode 118, and thus the feedback, similarly affect diode 124 and the bias voltage. In the alternative, diode 124 may be replaced by a temperature sensitive element, such as a thermistor. It should be understood that the bias voltage appearing at the noninverting input of op amp 112 may be established at many different levels and by many different ways that are well known in the art.

The compensation signal generated by compensation circuit 110 is output from op amp 112 to both of amplifier circuits 130 and 170. Amplifier circuit 130 is typically comprised of dual gate FET amplifier 132 which has one gate (G_1) coupled through resistor 134 to the output of op amp 112 and through capacitor 136 to ground. The other gate (G_2) of FET 132 receives the input IF signal through variable capacitor 138, and is coupled to ground through the parallel combination of resistor 140, variable capacitor 142 and inductor 144. The source (S) of FET 132 is also coupled to ground through the parallel combination of resistor 146 and capacitor 148. The drain (D) of FET 132 is coupled to the supply voltage +VCC through the parallel combination of resistor 150 and inductor 152 while also being coupled to ground through variable capacitor 154. The drain (D) of FET 132 is coupled to the input of filter 160, which in the preferred embodiment is a surface acoustic wave (SAW) bandpass filter. SAW filter 160 typically has a center frequency at 70 MHz and a bandwidth of 1.25 MHz.

The voltage at gate (G_1) as determined by the output of op amp 112 controls the level of gain of FET 132. The input IF signal is amplified at the determined gain level by FET 132 with the output voltage appearing across the input transducer (not shown) of SAW filter 160. The parallel combination of resistor 150 and inductor 152 are of values selected such that, in combination with the output impedance of FET 132 appearing at the drain (D), the impedance of this circuit supplies the source impedance seen by SAW filter 160.

It may be shown that by using simple, tuned matching networks, the total insertion loss (IL) of the complete SAW filter is approximately:

$$IL = \left| \frac{2\,G_a\,G_s}{(G_a + G_s)^2} \right|^2 \qquad (1)$$

where:

Ga is the real part of the acoustic admittance; and

Gs is the real part of the source and load admittances.

Also, it may be shown that the triple transit response (TTR) of the complete filter is defined by:

$$TTR = \left| \frac{2\,G_a\,G_s}{(G_a + G_s)^2} \right|^2 \cdot \left| \frac{G_a^2}{(G_a + G_s)^2} \right|^2 \qquad (2)$$

Using the relationships set forth by equations (1) and (2), one can compute that for a triple transit response of 30 dB, relative to the main signal, an insertion loss of 12 dB can be achieved.

Amplifier circuit 170 is constructed in a manner similar to that of amplifier circuit 130. Amplifier circuit 170 is comprised of dual gate FET amplifier 172, preferably the same as FET 132, which has one gate (G_1) coupled

through resistor 174 to the output of op amp 112 and through capacitor 176 to ground. The other gate (G_2) of FET 172 is coupled to the output of SAW filter 160 for receiving the filtered and amplified IF signal the output therefrom, and is coupled to ground through the parallel combination of resistor 180, variable capacitor 182 and inductor 184. The source (S) of FET 172 is also coupled to ground through the parallel combination of resistor 186 and capacitor 188. The drain (D) of FET 172 is coupled to the supply voltage +VCC through the parallel combination of resistor 190 and inductor 192 while also being coupled to ground through variable capacitor 194. The output of FET 172 is provided through variable capacitor 196 also coupled to the drain (D) of FET 172.

The voltage at gate (G_1), as determined by the output of op amp 112, again controls the level of gain of FET 172. The IF signal output from SAW filter 160 is amplified at the determined gain level by FET 172 with the output voltage appearing at the output of variable capacitor 196. The parallel combination of resistor 180 and inductor 182 are of values selected such that, in combination with the input impedance of FET 172 appearing at the gate (G_2), the impedance of this circuit provides the proper load for the output impedance of SAW filter 160.

The IF signal output from amplifier 170 is provided as an input to downconverter 20. In FIG. 2B, portions of downconverter 20 are illustrated in further detail. The IF signal is provided as an input to a mixer FM IF system 200 through a balanced input network comprised of capacitors 202, 204 and 206 and variable inductor 208. System 20 in the preferred embodiment is a high performance monolithic low power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. Such a device is sold by Signetics Corporation of Sunnyvale, Calif. under Part No. NE/SA 605.

The input IF is provided through the balanced input network to two input ports of mixer 210. A third input port receives a lower frequency IF reference signal provided by oscillator 212 through driver 214. Mixer 210 mixes the IF signal with the IF reference signal to provide a lower frequency IF signal which is output therefrom to filter 216. Filter 216 is a bandpass filter, typically a crystal filter, with removes out of band frequencies from the IF signal. The filtered IF signal is output from filter 216 to an input of IF amplifier 218.

Amplifier 218 includes a decoupling network comprised of capacitors 220 and 222 coupled thereto for proper IF decoupling. Amplifier 218 amplifies the IF signal and provides the amplified IF signal as an output through resistor 224 to filter 226. Filter 226 is again a bandpass filter, also typically a crystal filter, which removes out of band frequencies from the IF signal. The filtered IF signal is output from filter 226 to an input of IF amplifier 228.

The filtered IF signal output from filter 226 is also provided as an output to digital signal processing hardware (not shown) for demodulation and correlation of I and Q samples of the encoded digital data of which the IF signal is comprised when the received signals are CDMA signals. It is further envisioned that the signal output from filter may be further mixed with a lower frequency signal and filtered (by components of downconverter 20 not shown) to provide the user baseband signal for digital processing.

Amplifier 218 also provides an output of the amplified IF signal to a logarithmic received signal strength indicator, RSSI 228, which accurately measures the power of the IF signal over a 90 dB range. RSSI 228 provides an output of a linear signal, RSSI OUT, indicative of measured logarithmic signal power. The output of RSSI 228 is coupled to the noniverting input of op amp 100 of integrator 22, while also being coupled to ground through parallel resistor 230 and capacitor 232. The RSSI OUT signal is thus provided as an output to integrator 22 where the AGC signal is generated as discussed above.

When telephone 10 is in the FM mode of operation, for dual mode telephones, the signal output from filter 226 is further processed as an FM signal and not a digital signal. The signal output from filter 226 is also coupled to an input of IF amplifier 234.

Filters 216 and 226 need to be wide passband filters for eliminating out of band frequencies in the CDMA mode of operation. However, additional filtering is required for the when telephone 10 is in the FM mode of operation. Thus, additional filters (not shown) need to be added to the filtering arrangement with these filters being of a narrow passband tuned to the designated RF channel to which telephone 10 is assigned for FM communications. It is envisioned that the additional filters would be selected from a bank of narrow passband filters in response to a filter selection signal corresponding to the FM channel of use. These additional filters may be switched into the circuit to provide additional filtering to that of filters 216 and 226, or having filters 216 and 226 switched out of the circuit with the appropriately selected additional filters from the bank of filters providing the necessary filtering.

Amplifier 234 also includes a decoupling network comprised of capacitors 236 and 238 coupled thereto for proper IF decoupling. Amplifier 234 amplifies the IF signal and provides the amplified IF signal as an output to quadrature detector 240. The other output of amplifier 234 is coupled to quadrature detector 240 and also AC coupled to a tuned quadrature network comprised of capacitors 242, 244, 246 and inductor 248. The output of quadrature detector 240 is coupled across parallel coupled resistor 250 and capacitor 252 as the audio signal, UNMUTED AUDIO.

Quadrature detector 240 also provides an output to mute switch 254. Mute switch 254 also has an input for receiving a control signal, MUTE IN, which controls whether the audio output therefrom is muted or unmuted. The output of mute switch 254 is coupled across parallel coupled resistor 256 and capacitor 258 as the audio signal, MUTED AUDIO.

It can be seen from the FIGS. 2A and 2B, analog circuitry may be used to provide closed loop automatic gain control in the processing of both analog (FM) and digital (CDMA) signals. Such a circuit implementation eliminates the necessity to have both analog and digital circuitry in a dual mode signal processing environment. Furthermore, the use of analog techniques in gain control of digital signals provides for faster gain control than over conventional techniques.

The circuit of the present invention provides for a low cost, low power implementation of an automatic gain control circuit for various radio designs. Having accurate measurement of signal strength and linear control over gain over a relatively large bandwidth, typi-

cally in excess of 80 dB, the circuit is particularly applicable to the CDMA cellular environment where gain control is a critical element in the CDMA telephone. The advantages of the present invention overcome many of the deficiencies of other techniques for gain control, particularly those experienced in the cellular telephone environment.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

We claim:

1. A closed loop automatic gain control (AGC) circuit comprising:

a first amplifier having a signal input, a gain control input and an output, said first amplifier signal input capable of receiving an input signal;

a filter having an input and an output, said filter input coupled to said first amplifier output; and

a second amplifier having a signal input, a gain control input and an output, said first amplifier signal input coupled to said filter output;

a received signal strength indicator having an input coupled to said second amplifier output, and an output;

an integrator having a pair of inputs and an output, one of said integrator inputs capable of receiving a reference signal and another one of said integrator inputs coupled to said received signal strength indicator output;

a compensation circuit having an input coupled to said integrator output, and an output coupled to said first and second amplifier gain control inputs.

2. The circuit of claim 1 wherein said first and second amplifiers are variable gain amplifiers having a gain determined by a compensated gain control signal provided by said compensation circuit at said first and second amplifier gain control inputs.

3. The circuit of claim 1 wherein said compensation circuit comprises:

an op amp having a noninverting input capable of receiving a reference voltage, an inverting input capable of receiving an uncompensated gain control signal provided by said integrator, and an output; and

a nonlinear feedback network coupled between said op amp output and said inverting input.

4. The circuit of claim 1 wherein said integrator comprises:

an op amp having a noninverting input capable of receiving a measurement signal provided by said received signal strength indicator, and an inverting input capable of receiving said reference signal, and an output; and

a capacitive feedback network coupled between said op amp output and said inverting input.

5. The circuit of claim 1 wherein said received signal strength indicator comprises measurement means for, receiving an input signal from said second amplifier, measuring logarithmic power of said input signal, and providing a corresponding a corresponding linear uncompensated gain control signal.

6. The circuit of claim 5 wherein said received signal strength indicator further comprises:

frequency conversion means for translating the frequency of said input signal to a lower frequency;

filter means for filtering undesired frequency components from said input signal; and

amplifier means for amplifying said input signal at a predetermined gain.

7. The circuit of claim 1 wherein:

said first and second amplifiers each comprise a FET amplifier each having first and second gates, and a drain, each of said first and second amplifier FET amplifier first gate forming a respective first and second amplifier gain control input, each of said first and second amplifier FET amplifier second gate each forming a respective first and second amplifier signal input, and each of said first and second amplifier FET amplifier drain forming a respective first and second amplifier output; and

said filter comprises a bandpass filter.

8. The circuit of claim 7 wherein said bandpass filter comprises a surface acoustic wave filter.

9. The circuit of claim 7 wherein said compensation circuit comprises:

a first op amp having a noninverting input capable of receiving a reference voltage, an inverting input capable of receiving an an uncompensated gain control signal provided by said integrator, and an output; and

a nonlinear feedback network coupled between said first op amp output and said first op amp inverting input.

10. The circuit of claim 9 wherein said integrator comprises:

a second op amp having a noninverting input capable of receiving a measurement signal provided by said received signal strength indicator, and an inverting input capable of receiving said reference signal, and an output; and

a capacitive feedback network coupled between said second op amp output and said second op amp inverting input.

11. The circuit of claim 1 wherein said received signal strength indicator comprises measurement means for, receiving an input signal from said second amplifier, measuring logarithmic power of said input signal, and providing a corresponding a corresponding linear uncompensated gain control signal.

12. A closed loop automatic gain control (AGC) circuit comprising:

amplifier means for receiving an input signal which is susceptible to variations in signal power, receiving a control signal, amplifying said input signal at a gain level determined by said control signal and providing a corresponding amplifier means output signal, said amplifier means comprising:

compensation means for receiving said control signal and generating a corresponding compensation signal according to predetermined compensation characteristics;

input amplification means for, receiving an input signal and said compensation signal, amplifying said input signal at an input gain level determined by said compensation signal and providing a corresponding input amplification means output signal;

filter means for receiving and filtering said input amplification means output signal; and

output amplification means for, receiving said filtered input amplification means output signal and said compensation signal, amplifying said filtered input amplification means output signal at an output gain level determined by said compensation signal and providing a corresponding output amplification means output signal as said amplifier means output signal;

measurement means coupled to said amplifier means for measuring logarithmic signal power of said amplifier means output signal and providing a corresponding linear measurement signal; and

integration means for receiving said measurement signal, receiving a reference signal which corresponds to a desired signal power of said output signal, integrating with respect to time a difference between said measurement signal and said reference signal, and providing said control signal.

13. The circuit of claim 12 wherein said measurement means comprises a received signal strength indicator circuit.

14. The circuit of claim 12 wherein said integration means comprises:

an op amp having a noninverting input capable of receiving said measurement signal and an inverting input capable of receiving said reference signal, and an output; and

a capacitive feedback network coupled between said op amp output and said inverting input.

15. The circuit of claim 13 wherein said integration means comprises:

an op amp having a noninverting input capable of receiving said measurement signal and an inverting input capable of receiving said reference signal, and an output; and

a capacitive feedback network coupled between said op amp output and said inverting input.

16. The circuit of claim 12 wherein said input amplification means and said output amplification means each comprise a dual gate FET amplifier.

17. The circuit of claim 12 wherein:

said compensation means generates said compensation signal according to predetermined gain compensation characteristics; and

said input amplification means and said output amplification means gain in dB is a linear function of said control signal over a predetermined gain range.

18. The circuit of claim 12 wherein said input signal contains information in a predetermined one of digital and analog form.

19. A method for providing closed loop automatic gain control over a high dynamic range comprising the steps of:

compensating a control signal according to predetermined compensation characteristics so as to provide a compensated control signal;

amplifying an input signal at a gain determined by said compensated control signal, said amplification of said input signal comprising the steps of:

receiving said input signal;

receiving said compensated control signal;

amplifying said input signal at a first gain level determined by said compensated control signal;

providing a first amplified signal corresponding to said first gain level amplified input signal;

filtering said first amplified signal;

amplifying said filtered first amplified signal at a second gain level determined by said compensated control signal; and

providing an output signal corresponding to said second gain level amplified filtered first amplified signal;

measuring log signal power of said output signal;

providing a measurement signal corresponding to measured signal power of said output signal;

integrating with respect to time a difference between said measurement signal and a reference signal; and

providing said control signal corresponding to a result of integrating said measurement signal and reference signal difference.

20. The method of claim 11 wherein said compensation characteristics are gain characteristics.

21. The method of claim 11 wherein said measurement signal is a linear signal corresponding to said measured log signal power.

22. The method of claim 14 wherein said step of filtering comprises bandpass filtering said first amplified signal.

* * * * *

EXHIBIT F.

US005099204A

United States Patent [19]

Wheatley, III

[11] Patent Number: 5,099,204

[45] Date of Patent: Mar. 24, 1992

[54] LINEAR GAIN CONTROL AMPLIFIER

[75] Inventor: Charles E. Wheatley, III, Del Mar, Calif.

[73] Assignee: Qualcomm Incorporated, San Diego, Calif.

[21] Appl. No.: 598,845

[22] Filed: Oct. 15, 1990

[51] Int. Cl.[5] H03G 3/30

[52] U.S. Cl. 330/279; 330/306; 330/310

[58] Field of Search 330/277, 278, 279, 285, 330/302, 305, 306, 310; 455/219, 234, 240, 241

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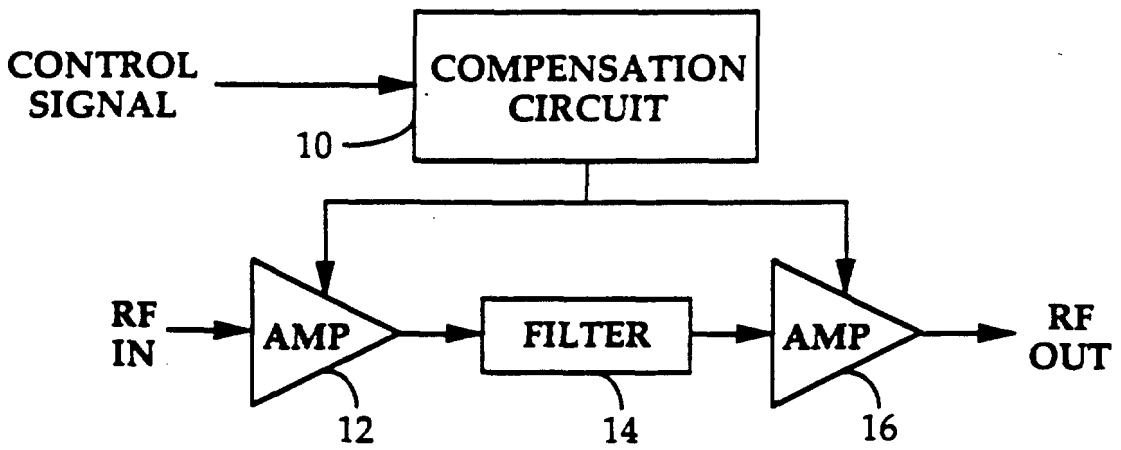
Primary Examiner—Steven Mottola

Attorney, Agent, or Firm—Russell B. Miller

[57] ABSTRACT

An amplification circuit having a compensation circuit for receiving a control signal and generating a corresponding compensation signal according to predetermined compensation characteristics. An input amplification circuit is provided for, receiving an input signal and the compensation signal amplifying the input signal at an input gain level determined by the compensation signal and providing a corresponding input amplification circuit output signal. A filter element receives and filters unwanted frequency components from the input amplification circuit output signal. An output amplification circuit is provided for, receiving the filtered input amplification circuit output signal and the compensation signal, amplifying the filtered input amplification circuit output signal at an output gain level determined by the compensation signal and providing a corresponding output amplification circuit output signal.

19 Claims, 2 Drawing Sheets



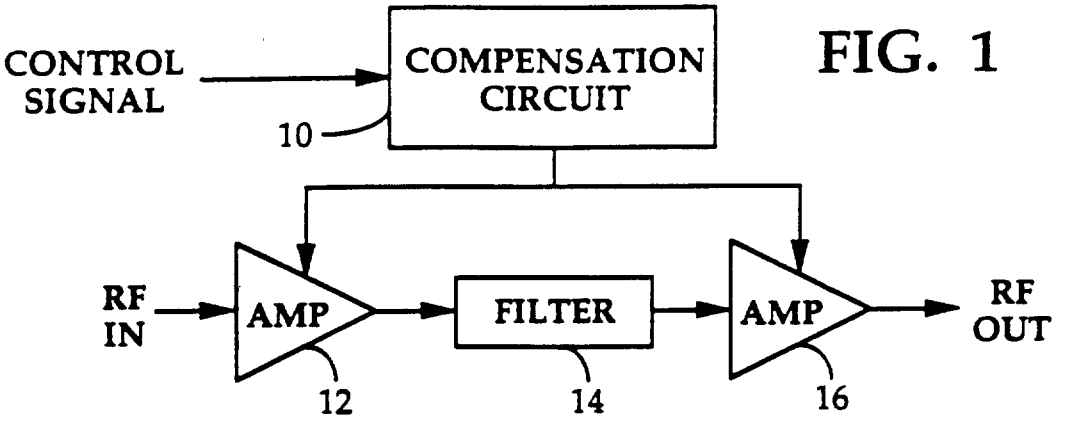


FIG. 1

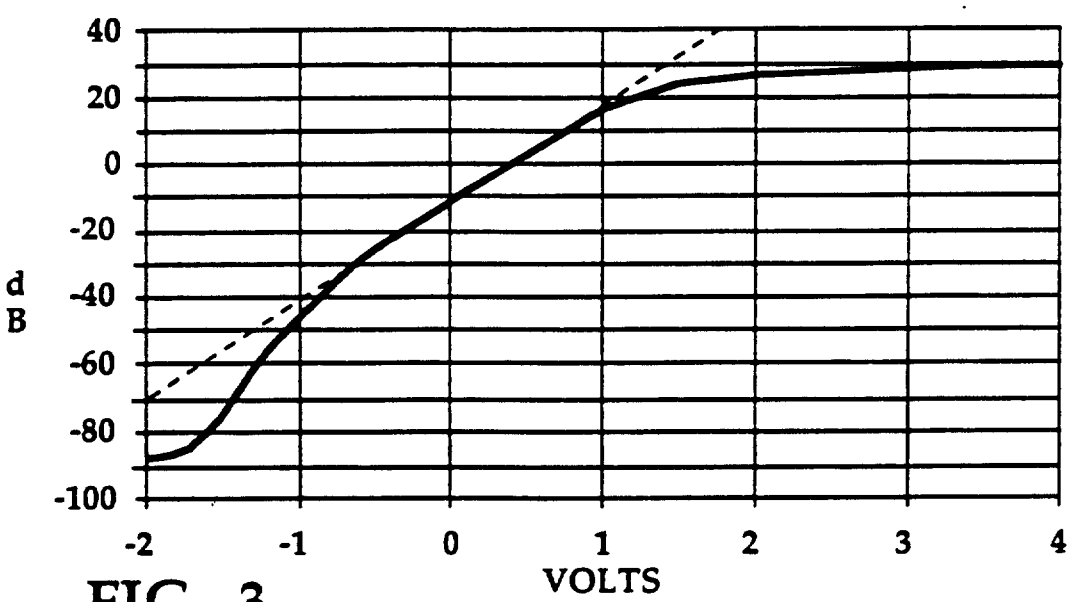


FIG. 3

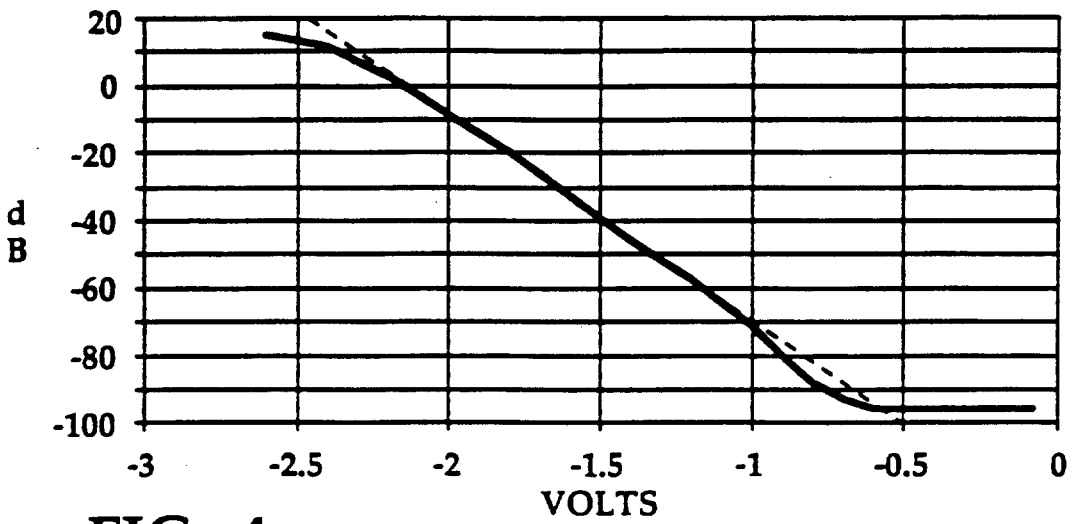


FIG. 4

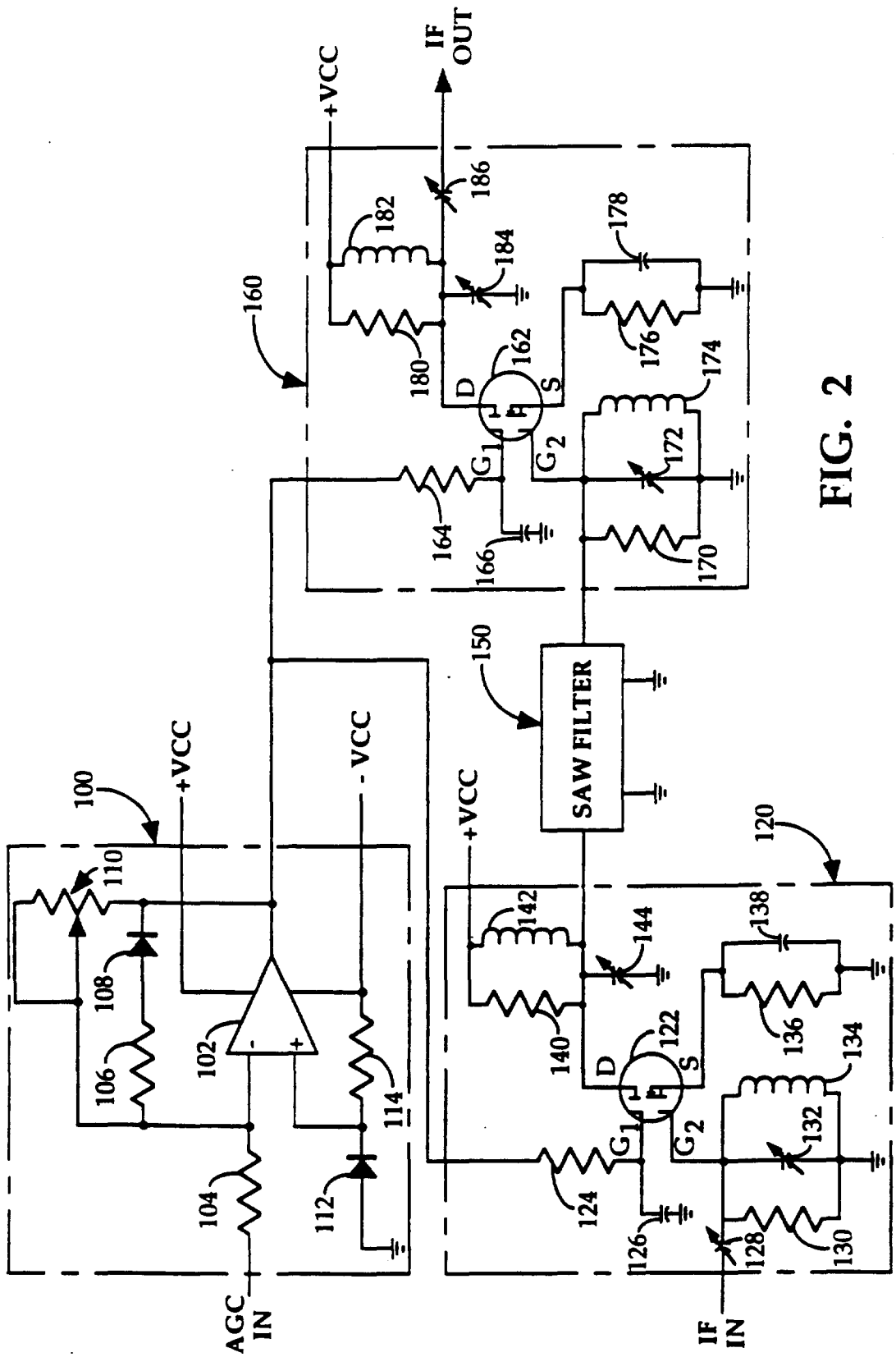

IF OUT
+VCC
160
182
186
184
178
180
162
D
S
176
174
G1
G2
172
164
166
170
150
SAW FILTER
100
+VCC
- VCC
110
108
106
102
114
104
112
AGC IN
+VCC
120
142
144
138
140
122
136
134
132
124
126
128
130
IF IN

FIG. 2

LINEAR GAIN CONTROL AMPLIFIER

BACKGROUND OF THE INVENTION

I. Field of the

The present invention relates to amplifiers. More particularly, the present invention relates to a novel and improved radio frequency amplifier circuit which provides linear control of gain, when such gain is measured in decibels, over a large gain range.

II. Description of the Related Art

The use of automatic gain control (AGC) circuits to control amplifier gain in communication terminals has been accomplished by many various designs. Typically the range in gain for such amplifiers is somewhat limited, and therefore are not directly useful in applications where a very large dynamic range of signals are to be accommodated.

In applications where a surface acoustic wave (SAW) filter is utilized in the receiver for band filtering, special care must be taken in choosing the impedance of the circuit seen by the SAW filter. Traditionally the SAW filter is matched in impedance with the external circuit by using simple series coupled inductors at the input and output of the SAW filter. Such simple impedance matching provides for a reduction of the well known phenomena of triple transit interference (reflections of the signal of interest within the SAW filter). However, such a reduction in triple transit is at the expense of increased insertion losses.

A typical insertion loss using a conventionally configured SAW filter is approximately 20 dB. The minimum insertion loss that a simple SAW filter is theoretically capable of producing is 6 dB. However, at the minimum insertion loss the triple transit signal is at a level that can substantially interfere with a signal of interest.

In applications requiring a large gain control, and which also utilizes SAW filters for band filtering, the loss of the SAW filter should be minimized if one is to maximize the effective range of controllable gain.

In certain applications, such as in CDMA cellular telephone transceivers where transmitter power control and receiver AGC are essential to system operation, the transmitter and receiver must both operate over a relatively high dynamic range and track each others gain change over the full range of control. In such an environment, the receiver can be required to operate over a gain range that can easily reach as high as 80 dB.

In many systems, again such as in CDMA cellular telephone transceivers, it is essential that in response to a received signal, the AGC loop should provide a signal indicative of measured signal strength which is linear, in terms of output indication as a function of dB of input. Conventional AGC circuits normally exhibit such a characteristic over only a portion of the full control range, due to nonlinearities in the gain control function of the amplifier.

It is therefore an object of the present invention to provide a novel and improved amplification circuit which, in response to a gain control signal, is capable of substantially linear gain control operation over a relatively large range.

It is another object of the present invention to provide an amplifier circuit in which gain in dB is controlled as a linear function of an input control signal.

It is yet another object of the present invention to provide active impedance matching of a SAW filter to minimize insertion loss at specified levels of triple transit signals.

It is still a further object of the present invention to provide a temperature compensated amplification circuit capable of substantially linear gain control over a large dynamic range over a wide temperature range.

SUMMARY OF THE INVENTION

The present invention is a novel and improved automatic gain control circuit controlled linear amplifier capable of linear operation over a relatively large range of gains. The amplifier of the present invention involves the utilization of two low-cost amplifiers, typically dual gate FET amplifiers, appropriately mismatched to a filter, specifically a SAW bandpass filter as a signal amplification circuit. The amplifier of the present invention further involves the utilization of a low frequency amplifier, typically an operational amplifier (op-amp), with diode feedback to provide linear gain control and temperature compensation for the signal amplification circuit over a gain operational range of over 110 dB.

In accordance with the present invention an amplifier circuit is disclosed which is capable of providing linear gain control over a high dynamic range. The circuit comprises in an exemplary embodiment a compensation circuit, a first amplifier, a filter and a second amplifier.

The compensation circuit receives a linear control signal corresponding to a log power measurement of a received signal. The compensation circuit is responsive to the control signal for generating, a corresponding nonlinear control signal, or compensation signal, according to predetermined compensation characteristics. The first amplifier is coupled to the compensation circuit for receiving the compensation signal and for receiving an input RF signal. The first amplifier amplifies the input RF signal at an input gain level determined by the compensation signal so as to provide a corresponding first amplifier output signal.

The filter is coupled to the first amplifier so as to receive the first amplifier output signal. The filter removes unwanted frequency components from the first amplifier output signal and provides a filtered first amplifier output RF signal.

The second amplifier is also coupled to the compensation circuit for receiving the compensation signal and to the filter for receiving the filtered first amplifier output signal. The second amplifier amplifies the filtered first amplifier output signal at an output gain level determined by the compensation signal so as to provide a corresponding second amplifier output RF signal.

The filter has an input and output impedance that is mismatched by the first and second amplifiers to provide a reduction in insertion loss at a predetermined triple transit level. The compensation circuit compensates for inherent device nonlinearities in gain, for a linear control signal, of the first and second amplifiers over the large dynamic range of operation required. The compensation circuit also provides for temperature compensation of the first and second amplifiers so as to reduce the adverse affects of changes in temperature on gain.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

FIG. 1 is a block diagram of an exemplary embodiment of the linearized automatic gain control amplifier of the present invention:

FIG. 2 is an exemplary schematical circuit diagram of the linearized automatic gain control amplifier of FIG. 1:

FIG. 3 is a graph illustrating the inherent gain characteristic of the uncompensated amplifier circuit used in the embodiment of FIG. 2; and

FIG. 4 is a graph illustrating the linearized gain characteristic of the compensated amplifier circuit used in the embodiment of FIG. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings, FIG. 1 illustrates in block diagram form an exemplary embodiment of the linear amplification circuit of the present invention. The typical environment in which the circuit of FIG. 1 is implemented is in an automatic gain control (AGC) circuit.

The use of AGC circuits are well known in the communications art for receivers or transceivers operating in the RF frequency band. AGC circuits are typically used for, based upon the strength of the received signal, controlling the power of a received signal for later processing of the signal and also for controlling transmitter power. In the AGC circuit, a measurement of signal strength, or power, of the received signal is performed at some other point where an AGC signal is generated. The AGC signal is typically provided as a gain control signal to a variable gain amplifier. The amplifier in response to the AGC signal adjusts the amount of gain applied to the received signal. The amplifier gain may be negative or positive depending upon system parameters and signal strength.

The amplification circuit of FIG. 1 is comprised of compensation circuit 10, variable gain amplifier circuit 12, filter 14 and variable gain amplifier circuit 16. In FIG. 1, a gain control signal is provided to compensation circuit 10. In an AGC application, such a control signal is generated by a signal strength measurement circuit (not shown) in linear correspondence with the log of the measured signal strength of the received RF signal, or corresponding IF signal if frequency downconverted before measurement.

The control signal is provided as an input to compensation circuit 10 where the control signal is modified according to predetermined compensation characteristics. Compensation circuit 10 provides compensation in the control signal for inherent nonlinearities in the amplification circuitry used to amplify the input RF signal, corresponding to the received RF signal. Compensation circuit 10 thus generates a compensated control signal which is output therefrom as a nonlinear control signal or compensation signal. It should be understood that the compensation signal is typically linear with respect to the control signal, except for those portions of the gain curve for the amplifier circuits where nonlinearities occur in response to a linear control signal.

In a CDMA mobile telephone, the amplification circuitry is required to operate over a high dynamic range, such as in excess of 80 dB. The amplification circuitry employed in this application must be low in cost for maximum commercial exploitation. Such a low cost design employs amplifier components which can experience nonlinearities in gain when conventional techniques are used in gain control over a large operational gain range. For proper operation of the mobile telephone at such a large operational gain range, compensation must be provided. Accurate gain control is particularly critical if pairs of gain controlled elements are to be used. In such an application, gain controlled amplifiers are used in both the receiver and transmitter and must track each other with respect to gain variation or adjustment.

In the exemplary embodiment, a cascaded amplifier scheme is used to provide variable gain control in amplification of the received signal. Disposed between the cascaded amplifiers is a filter which removes out of band frequency components from the RF signal. The dual amplifiers also serve to provide active impedance matching of the filter.

As illustrated in FIG. 1, amplifier circuits 12 and 14 both receive, at a respective gain control input, the compensation signal from compensation circuit 10. Amplifier circuit 12 receives the RF signal at an input and amplifies the signal at a gain level as determined by the compensation signal. The amplified signal is output from an output of amplifier circuit 12 signal as a input to filter 14.

Filter 14 is typically a bandpass filter, although other filter types may be used depending on the frequency plan. In the mobile telephone application, filter 14 may be implemented as a SAW filter. Filter 14 removes unwanted frequency components from the RF signal. Filter 14 provides the filtered signal at an output thereof to an input of amplifier circuit 16. Amplifier circuit 16 receives the filtered RF signal at an input and amplifies the signal at a gain level as determined by the compensation signal.

Filter 14 implemented as a SAW filter has an inherent input and output impedance that must be properly mismatched to provide a minimum insertion loss at a level of tolerable triple transit. Typically SAW filters employ a passive component, such as an inductor, at the input and output to provide the proper impedance matching to translate the filter impedance to a value appropriate for coupling to 50Ω circuit elements. However, such impedance matching techniques result in insertion losses much greater than the theoretical minimum 6 dB, and typically on the order of 20–25 dB to avoid problems caused by the triple transit effect. In using a cascaded amplifier arrangement, amplifier circuits 12 and 16 provide "active" impedance matching which enables maximum reduction of insertion loss to a level which has a tolerable triple transit effect. Insertion losses can thus be readily achieved in the more optimum range of 14–15 dB.

FIG. 2 illustrates in further detail an exemplary embodiment of the amplification circuit of FIG. 1. Compensation circuit 100 receives an AGC signal and in response thereto generates the appropriate compensation. The resulting compensation signal is output from compensation circuit 100 to both amplifier circuits 120 and 160.

Amplifier circuit 120 receives and amplifies an input IF signal at a gain level determined by the compensation signal. The amplified IF signal is then output to filter 150 where it is bandpass filtered and output to amplifier circuit 160. Amplifier circuit 160 receives the amplified and filtered IF signal where amplified at a gain level determined by the compensation signal. The amplified IF signal is then output from amplifier circuit 160 for further processing.

Compensation circuit 100 is comprised of an operational amplifier, op amp 102, which has an inverting

input coupled to receive the AGC signal through input resistor **104**. The inverting input is also coupled to the output of op amp **102** through a nonlinear feedback circuit comprised of series coupled resistor **106** and diode **108** which are coupled in parallel with variable resistor **110**. The noninverting input of op amp **102** is provided with a reference or bias voltage across diode **112** that is provided through resistor **114** from the supply voltage −VCC. Resistors **104**, **106** and **114** are typically of the same resistance, e.g., 10 KΩ value, while variable resistor **110** is capable or providing a much larger resistance value, e.g. 50 KΩ.

In the operation of compensation circuit **100**, when the AGC voltage is above the bias voltage appearing at the noninverting input of op amp **102**, the parallel resistance combination of resistor **106** and variable resistor **110**, along with input resistor **104** (R106||R110/R104) set a first slope gain curve for operation of op amp **102**. When the AGC voltage is below the bias voltage, the value of variable resistor **110** along with input resistor **104** (R110/R104) set a second, and different, gain curve for operation of op amp **102**. Furthermore diodes **108** and **114** are preferably of the same type such that changes in temperature affecting diode **108**, and thus the feedback, similarly affect diode **114** and the bias voltage. In the alternative, diode **114** may be replaced by a temperature sensitive element such as a thermistor. It should be understood that the bias voltage appearing at the noninverting input of op amp **102** may be established at many different levels and by many different ways that are well known in the art.

The compensation signal generated by compensation circuit **100** is output from op amp **102** to both of amplifier circuits **120** and **160**. Amplifier circuit **120** is typically comprised of dual gate FET amplifier **122** which has one gate (G_1) coupled through resistor **124** to the output of op amp **102** and through capacitor **126** to ground. The other gate (G_2) of FET **122** receives the input IF signal through variable capacitor **128**, and is coupled to ground through the parallel combination of resistor **130**, variable capacitor **132** and inductor **134**. The source (S) of FET **122** is also coupled to ground through the parallel combination of resistor **136** and capacitor **138**. The drain (D) of FET **122** is coupled to the supply voltage +VCC through the parallel combination of resistor **140** and inductor **142** while also being coupled to ground through variable capacitor **144**. The drain (D) of FET **122** is coupled to the input of SAW filter **150**.

The voltage at gate (G_1) as determined by the output of op amp **102** controls the level of gain of FET **122**. The input IF signal is amplified at the determined gain level by FET **122** with the output voltage appearing across the input transducer (not shown) of SAW filter **150**. The parallel combination of resistor **140** and inductor **142** are of values selected such that, in combination with the output impedance of FET **122** appearing at the drain (D), the impedance of this circuit supplies the source impedance seen by SAW filter **150**.

It may be shown by using simple, tuned matching networks, the total insertion loss (IL) of the complete SAW filter is approximately:

$$IL = \left| \frac{2G_aG_s}{(G_a + G_s)^2} \right|^2 \quad (1)$$

where:

Ga is the real part of the acoustic admittance: and

Gs is the real part of the source and load admittances.

Also, it may be shown that the triple transit response (TTR) of the complete filter is defined by:

$$TTR = \left| \frac{2G_aG_s}{(G_a + G_s)^2} \right|^2 \cdot \left| \frac{G_a^2}{(G_a + G_s)^2} \right|^2 \quad (2)$$

Using the relationships set forth by equations (1) and (2), one can compute that for a triple transit response of 30 dB, relative to the main signal, an insertion loss of 12 dB can be achieved.

Amplifier circuit **160** is constructed in a manner similar to that of amplifier circuit **120**. Amplifier circuit **160** is is comprised of dual gate FET amplifier **162**, preferably the same as FET **122**, which has one gate (G_1) coupled through resistor **164** to the output of op amp **102** and through capacitor **166** to ground. The other gate (G_2) of FET **162** is coupled to the output of SAW filter **150** for receiving the filtered and amplified IF signal the output therefrom, and is coupled to ground through the parallel combination of resistor **170**, variable capacitor **172** and inductor **174**. The source (S) of FET **162** is also coupled to ground through the parallel combination of resistor **176** and capacitor **178**. The drain (D) of FET **162** is coupled to the supply voltage +VCC through the parallel combination of resistor **180** and inductor **182** while also being coupled to ground through variable capacitor **184**. The output of FET **162** is provided through variable capacitor **186** also coupled to the drain (D) of FET **162**.

The voltage at gate (G_1), as determined by the output of op amp **102**, again controls the level of gain of FET **162**. The IF signal output from SAW filter **150** is amplified at the determined gain level by FET **162** with the output voltage appearing at the output of variable capacitor **186**. The parallel combination of resistor **170** and inductor **172** are of values selected such that, in combination with the input impedance of FET **162** appearing at the gate (G_2), the impedance of this circuit provides the proper load for the output impedance of SAW filter **150**.

In should be noted that the output impedance of a FET is typically greater than the input impedance. In amplifier circuit **120**, resistor **140** is used to set the output impedance of the circuit to match the input of SAW filter **150**. In amplifier circuit **160**, resistor **170** is used to set the input impedance of the circuit to match the output impedance of SAW filter **150**. The value of resistor **170** is lower in value than resistor **140** since the input impedance of the FET is greater than its output impedance. This mismatch in amplifier selected resistor values provides compensation for the difference in FET input and output impedance for impedance matching to any circuit element. In the embodiment shown herein, the resistors largely set the impedances with variations in FET impedances are not critical. It is further envisioned that more gain could be realized using transformer matching techniques.

FIG. 3 illustrates in graphical form the gain characteristics of the amplifier circuit without compensation of the AGC signal. The solid line and the dashed line respectively represent the actual gain characteristic curve and the desired gain characteristic curve. The circuit has straight line control of gain in dB for gain

values from about −40 dB to about 20 dB. The uncompensated amplifier circuit thus provides an operational region of 60 dB, where gain in dB is a linear function of the input voltage applied to the gain control input of the amplifiers. In the region below −40 dB, the actual gain departs quite radically from the desired straight line desired gain curve. It is this region below −40 dB which the present invention predominantly seeks to provide an improved correlation to the desired gain characteristic curve.

FIG. 4 illustrates in graphical form the gain characteristics of the amplifier circuit with compensation of the AGC signal. The solid line and the dashed line again respectively represent the actual gain characteristic curve and the desired linear gain characteristic curve. The circuit has straight line control of gain in dB for gain values from about −75 dB to about 10 dB. The compensated amplifier circuit thus provides an operational region of operation of about 85 dB, where gain in dB is a linear function of the input voltage applied to the gain control input of the amplifiers. In the region below −75 dB, the actual gain is markedly closer to the desired straight line gain curve than for the uncompensated circuit. It is therefore readily be seen that by providing a compensated AGC signal in the amplifier circuit of the present invention that an extended range of gain control in dB, which is a linear function of the input AGC signal, is possible.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

I claim:

1. An amplification circuit for amplifying an input signal where signal gain in decibels (dB) is a linear function of a control signal comprising:

compensation means for receiving a control signal and generating a corresponding compensation signal according to predetermined gain compensation characteristics;

input amplification means for, receiving an input signal and said compensation signal, amplifying said input signal at an input gain level determined by said compensation signal and providing a corresponding input amplification means output signal, said input amplification means gain in dB being a linear function of said control signal over a predetermined gain range;

filter means for receiving and filtering said input amplification means output signal; and

output amplification means for, receiving said filtered input amplification means output signal and said compensation signal, amplifying said filtered input amplification means output signal at an output gain level determined by said compensation signal and providing a corresponding output amplification means output signal, said output amplification means gain in dB being a linear function of said control signal over said predetermined gain range.

2. The amplification circuit of claim 1 wherein:

said filter means has a predetermined input and output impedance:

said input amplification means is further for providing a selected output impedance so as to match said filter means input impedance; and

said output amplification means is further for providing a selected input impedance so as to match said filter means output impedance.

3. The amplification circuit of claim 1 wherein said filter means comprises a surface acoustic wave (SAW) filter.

4. The amplification circuit of claim 3 wherein said input and output amplification means each comprises a FET amplifier.

5. The amplification circuit of claim 4 wherein:

said filter has a predetermined input and output impedance;

said input amplification means FET amplifier has a predetermined output impedance matched to said filter input impedance; and

said output amplification means FET amplifier has a predetermined input impedance matched to said filter output impedance.

6. An amplifier circuit, for use with an automatic gain control (AGC) circuit which generates an AGC signal, for in response to said AGC signal providing gain control of an input signal over a high dynamic range, said gain control being a linear function of said AGC control signal comprising:

a compensation circuit having an input and an output, said compensation circuit capable of receiving said AGC signal at said compensation circuit input and modifying said AGC signal according to predetermined gain compensation characteristics so as to provide a modified AGC signal at said compensation circuit output;

a first amplifier having a pair of inputs and an output, one of said first amplifier inputs coupled to said compensation circuit output and another one of said first amplifier inputs capable of receiving said input signal, said first amplifier having portions of a gain range in decibels (dB) which are piecewise linear with respect to said AGC signal, and said first amplifier gain range linear with respect to said modified AGC signal;

a filter having an input and an output, said filter input coupled to said first amplifier output; and

a second amplifier having a pair of inputs and an output, one of said second amplifier inputs coupled to said compensation circuit output and another one of said second amplifier inputs coupled to said filter output, said second amplifier having portions of a gain range in dB which are piecewise linear with respect to said AGC signal, and said second amplifier gain range linear with respect to said modified AGC signal.

7. The circuit of claim 6 wherein said filter comprises a surface acoustic wave (SAW) bandpass filter.

8. The circuit of claim 6 wherein said first and second amplifiers each comprise a dual gate FET amplifier.

9. The circuit of claim 7 wherein said first and second amplifiers each comprise a dual gate FET amplifier.

10. The circuit of claim 9 wherein:

said first amplifier further comprises a first impedance matching circuit coupled to said first amplifier output for matching an input impedance of said filter for a predetermined level of triple transit response of said filter; and

said second amplifier further comprises a second impedance matching circuit coupled to said first amplifier other input for matching an output impedance of said filter for said predetermined level of triple transit response of said filter; and

wherein said filter has an insertion loss corresponding to impedance levels established by said first amplifier in combination with said first impedance matching circuit and said second amplifier in combination with said second impedance matching circuit.

11. The circuit of claim **6** wherein said compensation circuit comprises:

an operational amplifier having a noninverting input capable of receiving a reference voltage, an inverting input capable of receiving an AGC signal and an output; and

a nonlinear feedback network coupled between said operational amplifier output and said inverting input.

12. The circuit of claim **11** further comprising thermal compensation means coupled to said noninverting input for controlling the level of said reference voltage as applied to said noninverting input.

13. The circuit of claim **9** wherein said compensation circuit comprises:

an operational amp having a noninverting input capable of receiving a reference voltage, an inverting input capable of receiving an AGC signal and an output; and

a nonlinear feedback network coupled between said op amp output and said inverting input.

14. The circuit of claim **13** further comprising compensation means coupled to said noninverting input for controlling the level of said reference voltage as applied to said noninverting input.

15. An method for amplifying over a high dynamic range an input signal where signal gain in decibels (dB) is a linear function of a control signal, said method comprising the steps of:

generating, in response to a linear control signal, a corresponding compensation signal according to predetermined gain compensation characteristics;

amplifying an input signal at an input gain level determined by said compensation signal and providing a corresponding first amplified signal, said first amplified signal being of a gain in dB which is a linear function of said control signal;

filtering said first amplified signal; and

amplifying said filtered first amplified signal at an output gain level determined by said compensation signal and providing a corresponding second amplified signal, said second amplified signal being of a gain in dB which is a linear function of said control signal.

16. The method of claim **15**, wherein said input signal is amplified by a first amplifier, said first amplified signal is filtered by a filter having a predetermined input and output impedance, and said filtered first amplified signal is amplified by a second amplifier, said method further comprising the step of providing impedance matching of said first and second amplifiers to said filter for a predetermined level of filter triple transit response.

17. The method of claim **15** wherein said step of generating said compensation signal comprises the steps of:

modifying said control signal according to a first gain compensation curve when said control signal is below a first predetermined level; and

modifying said control signal according to a second gain compensation curve when said control signal is above said first predetermined level.

18. The amplification circuit of claim **1** wherein said input and output amplification means each provide signal gain in dB as a first linear function of said control signal over a portion of said predetermined gain range and as a second linear function of said control signal over gains exceeding said predetermined gain range portion, said compensation means modifying said control signal corresponding to input and output amplification means gains exceeding said predetermined gain range.

19. The circuit of claim **6** wherein said first and second amplifiers are responsive to said modified AGC signal for providing a signal gain in dB over said gain range which is in linear correspondence with said AGC signal.

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EXHIBIT G.