RECEIVED

JAN 14 1993

FEDERAL COMMUNICATIONS COMMISSION
OFFICE OF THE SECRETARY

FILE COPY ORIGINAL

87-268

Report of the Specialist Group 6 to the FCC ACATS SS.WP3

DOCKET FILE COPY ORIGINAL

Advanced Television Receiver Cost

Prepared by

Werner F. Wedam,
for SG6

October 1992

Table of contents:

0. Executive Summary
1. Introduction
2. The Specialist Group
3. Assumptions
4. HDTV Receiver System Comparison Chart
5. HDTV Receiver Cost Table
6. Receiver Retail Price
7. Conclusion

Supporting documents:

- Receiver System Comparison Chart
- Receiver Cost Table

No. of Copies rec'd 2 Copies
List A B C D E

Advanced Television Receiver Cost

0. Executive Summary

SS /WP3 formed the Specialist Group 6 (SG6) to evaluate receiver cost in response to requests from the Advisory Committee for Advanced Television Service of the FCC (ACATS). Estimates for the cost of receivers for Advanced Television for the year 1998 were expected, when 1% market penetration of HDTV was assumed. SG6 requested information from the ATV Systems Proponents with the help of questionnaires and developed comparison tables from the data which was supplied by the proponents. The first table was a comparison of the technical complexity of the hardware for receivers of each system and the second table was a detailed comparison of the cost of that hardware.

SG6 conducted many telephone conferences and two face to face meetings. Much of the data was gathered before the first face to face meeting and at the meetings any disagreements were discussed and corrections to the tables were made.

In the course of this study great attention was paid to arrive at realistic cost figures for all receiver components. SG6 attempted to uncover the differences in complexity of the decoders of the proposed systems and to convert these differences into meaningful cost. SG6 recognized the inherent similarity of the processing in the all digital systems but also found that the cost of the display would have a major impact on HDTV receiver cost because in the foreseeable future it would be substantially higher than the cost of other materials.

The following is a summary of the key results of this report:

There is a difference between the cost of electronics for the proposed systems but its impact on receiver cost is virtually insignificant and the differences are smaller than the margin of error of this investigation.

The cost of the electronics which is different for all systems will decrease rapidly with volume and time, reducing the difference between systems even further.

The cost of the display is the same for all systems and has a substantial impact on the cost of HDTV and will not reduce appreciably in the near future.

SG6 mainly developed cost estimates for materials. Using a simple multiplier of 2.5, which may not be correct for all manufacturers, the following crude estimates for HDTV Receiver selling prices were obtained.

34" CRT type HDTV receivers could retail for around $2550.

56" HDTV projectors could retail for around $3850.

Advanced Television Receiver Cost

1. Introduction:

1.1.Background

The EIA conducted surveys to determine the cost of Advanced Television Receivers since 1988. A first report of a manufacturers' survey was issued in early 1989. Since the first survey several proposed HDTV systems were either withdrawn or changed and new all digital systems were announced. Because the old survey did not provide any useful information for the new systems, a new effort to estimate the cost of receivers for the proposed systems was started in 1991. The ATV Receiver Cost Specialist Group was formed in late 1991 as SG6 of the Working Party 3 of the Systems Subcommittee of the FCC Advisory Committee for Advanced Television Service (ACATS SS/WP3 SG6).

1.2.Purpose:

SG6 followed the guidelines of Working Party 3 to develop and report economic factors which could influence the selection of an HDTV system proposal for the next generation of television service for the United States. SS/WP3 researched the cost of production and delivery of HDTV, and SG6 researched the cost of receivers for HDTV.

The purpose of Specialist Group 6 (SG6) was to develop cost information for HDTV receivers and to estimate the range of selling price for such receivers, which could be used in HDTV market penetration studies by other subcommittees. An important result of this research was to show what the cost difference between receivers for the proposed systems is, and if such cost difference is substantial enough, that the decision for a system selection would be affected.

2. The Specialist Group

2.1 Membership

The members of the SG6 were representatives from the proponents as well as experts from companies with a sincere interest in the HDTV business, willing to support this process with time and effort. Mr. Ralph Justus was chairman of the group.

SG6 wishes to thank the many individuals who have contributed information and assistance in the process of this work.

2.2 SG6 Methodology

SG6 developed a receiver cost questionnaire which was sent to the proponents in January of 1992.

Although the responses provided answers to the questions in the questionnaire, the information was not in a suitable form for a comparison and to develop the desired cost estimate for the proposed systems. Much additional data was necessary to prepare a complete and meaningful cost prediction for HDTV receivers.

The HDTV Receiver System Comparison Chart (RSCC) was prepared with the data which was provided by the proponents. Because the responses to the questionnaire were not readily comparable the table was expanded with additional questions and an expected format for all entries was specified.

This expanded RSCC was sent to all members of SG6 and all proponents were asked to correct and complete their columns in the table. All responded with additions and corrections either by phone or in writing in preparation for the first face to face meeting of SG6 on 7/30/92 at the EIA office in Washington.

At the meeting the entries in the HDTV Receiver System Comparison Chart were discussed and corrections were suggested where necessary. A method to develop cost figures for the various entries in the table was proposed and agreed upon and an HDTV Receiver Cost Table (RCT) was started.

It was suggested to take the digital IC information provided by all proponents and enter it into the FAIRCOST II program for equivalent cost estimates. This program was developed for the IC industry and provides reasonably accurate cost predictions for ICs. The proponents agreed to this and also agreed to provide block diagrams, gate counts and pin counts for a suggested chip set for their systems. Those present at the meeting were satisfied that the cost of the digital chip sets could be estimated reasonably well by this method.

There was some concern whether the cost of the analog circuits and display could be estimated properly. It was generally recognized that the cost of the display would have a major impact on the cost of the receiver and that therefore the market study would be influenced by that cost more than by any other. As a result considerable effort was expended to find accurate estimates.

A copy of a draft report with completed charts and all attachments was mailed to the members of SG6 on 9/21/92 and finally reviewed at the second face to face

meeting on 10/05/92. At that meeting several uncertain estimates were discussed and a consensus was reached how to report them in the Specialist Group report. Subsequently, proponents had the opportunity for further adjustment and correction of their numbers.

2.3 Further supporting documents obtained by SG6 during the course of its work may be obtained from the chairman of SG6.

3. Assumptions:

The cost estimates could only yield useful results if certain assumptions about the performance, manufacturing volumes and a time frame for market penetration of HDTV could be agreed upon. It was assumed that the Specialist Group would receive sufficient technical detail information about each system to be able to understand the differences between systems and also to determine which components would be common for all HDTV systems.

3.1 Performance

Circuit complexity and cost of components was based on the performance of the system as tested and reported by the ATTC. Although manufacturers will be able to make their own decisions about the quality and performance of HDTV products they want to sell, using various cost/performance trade-off, SG6 could only estimate the cost of each system based on the performance as specified in the certification for testing and as actually tested (with the exception of a common assumption on equalizer range).

3.2 Time Frame of Estimate

Based on a systems selection in 1993 and subsequent field testing SG6 assumed 1998 as the time frame during which mass-production of HDTV receivers would start and sufficient volume would be achieved. This assumption was accepted by SS/WP3

3.3 Technology

The technology for the prototypes which were tested by the ATTC was substantially different from what would be used in mass production and no useful cost estimate could be developed using that circuitry or circuit packaging. Receiver cost was estimated consistent with predictions for improvements in key technologies such as displays, Integrated Circuits and Memories. For this cost study, second generation receiver designs were assumed which would utilize these

improved technologies, provided that their performance would be equivalent or better than the tested systems.

For the cost of ICs there is presently no reliable predictor for 1998 and therefore 1996 cost estimates were used, assuming .5μm CMOS technology for all digital IC's.

3.4 Production Volumes

To reach a 1% market penetration, 1 Million HDTV receivers would have to be built and that volume was assumed to be reached by the year 1998.

3.5 Double Conversion Tuners

The cost of the tuner and some parts of the IF were initially assumed the same for all HDTV systems. This decision was made after discussions with the proponents and study of a recent technical paper presented at the ICCE. Most tuner specifications are a function of system independent parameters such as the channel allocations, the transmitter power, expected service area, interference from other sources and the antenna used. The only specification which was considered system dependent was Local Oscillator Phase Noise. The proponents issued differing specifications for Local Oscillator Phase Noise (ranging form -60dBc/Hz to >-90dBc/Hz). Some argued that the 4VSB system is approximately as rugged as 16QAM and 32QAM required better specs and would cost more.

The cost of the tuner was therefore agreed to be $10 for standard phase noise requirements and $13 for a better phase noise specification.

3.6 Displays

The display performance, as specified by all proposed HDTV systems, is approximately described as 'double horizontal and double vertical' resolution compared to NTSC. Therefore all systems require the same CRT or projection optics and screen. For purposes of this investigation a CRT of 34W (W = Wide Screen) and a projector of 56W diagonal dimension and 16:9 aspect ratio were assumed. The 34W CRT has the same vertical height as a 27V conventional CRT and the 56W projector has the same vertical dimension as a 45V conventional projector.

The cost of future displays with various flat panel technologies and light-valve projectors could not be estimated with any degree of accuracy by SG6, because no such displays appear ready for consumer HDTV at this time. Therefore direct view

CRT and projector technology were assumed to be the most cost effective displays for the time frame of this analysis.

3.7 Scan circuitry

The scan circuitry is different between interlaced systems operating at 32 to 33kHz and progressive systems operating at 47kHz scan rates. Some suggested that this cost should be around $72 for progressive scan and provided some information about CRT displays at 48 kHz scan rates and higher, utilizing available power devices and other components. Others expressed serious concern that consumer displays at 47kHz were operating at substantially higher power levels than professional monitors and that more expensive technology might be required. The estimated cost premiums ranged from $12 to $50.

As a result of these discussions a cost for CRT deflection, power supply and video output of $60 was agreed to for interlaced systems and $73 for progressive scan systems ($13 premium for progressive scan). A similar approach was used to develop the cost for projector deflection ($25 premium).

3.8 Memory

The cost of memory in 16Mb size was at first considered common to all systems but the proponents provided information which in the case of CC-DigiCipher required 10ns access speeds and 20ns for DigiCipher. Some argued that such high speed memories will be expensive in the near future. The RCT table therefore projected a cost 40% higher than std. DRAM for high speed memory used in these systems. It is not clear yet if that projection is accurate because of insufficient cost information for this type of memory.

3.9 Other system independent common elements.

The cost of audio amplifiers and speakers, the cost of circuitry for NTSC processing and cabinets were assumed the same for all proposed systems.

4. HDTV Receiver Systems Comparison Chart (RSCC)

The RSCC can be found in the attachments.

The purpose of assembling the information in this table was to be able to evaluate the responses by the proponents side by side in the same format and to check if the information was suitable for comparison and sufficient for a cost estimate.

The information contained in the table was derived from the responses from the proponents and equivalent or similar information has been presented in the same

format for easy comparison. As can be seen, it is still difficult to compare the entries in this table because identical functions were designed quite differently. (e.g. Two proponents use the same Audio system with two totally different decoder designs).

This table was valuable to the members of SG6 to question the proponents about their system choices and to uncover real differences in requirements which could affect the system cost. On the other hand it also helped to understand where engineers had taken differing design approaches for functions which could be the same for two or more proposed systems without performance effects.

During the development of the RSCC an additional column was included which contained the format of the expected entry in each row of the table. This column helped a lot to make the information more suitable for cost comparison. Such information included, for instance, the size of ROM and RAM and the number of gates for each circuit function.

5. The HDTV Receiver Cost Table (RCT)

The RCT can be found in the attachments. The purpose for assembling the RCT was to combine function information from the RSCC into actual circuit blocks which could be built using the assumptions above and the cost of which could be estimated.

To provide sufficient information about each cost entry in the table, 'Remarks' are provided which contain key cost related information transferred from the RSCC. Proponents were also asked to provide functional block diagrams for circuit blocks and chip sets with information about IC chip areas and interconnections in addition to gate counts and bits of memory.

The cost data found in the RCT was developed in several ways depending on the receiver part in question.

5.1 Analog circuits common to all proponents: One or more proponents provided their own cost estimates and these cost estimates were accepted or modified after discussion by the members of SG6.

5.2 Digital circuits: Digital circuitry was described in terms of RAM, ROM and gates and IC pin count. The data was entered into the FAIRCOST II program which calculated the resulting cost.

5.3 Display circuitry. The cost of the CRT display circuitry was estimated using information from IDTV receivers, which are presently available and information from computer and professional monitors was also considered. These cost estimates were compared with estimates supplied by several proponents and for the case of interlaced scan good correlation was found between all estimates. For progressive scan for CRT and projectors, experts developed a compromise after considerable discussion.

5.4 Display cost:

CRT: The cost of the CRT was difficult to obtain because such cost is kept highly confidential by most manufacturers. For reference, the present cost of a 35" NTSC CRT, which is a little heavier than the 34" HDTV CRT used in the SG6 assumptions, is around $550. But the quality of the 34" CRT has to be higher to be suitable for HDTV, the finer mask is more expensive and the cost related to convergence and geometry goes up. Based on information from a major US manufacturer The following choice was given: 34" CRT with .7mm pitch @ $550 (NTSC quality), 34" CRT with .3mm pitch @ $1,000 (full HDTV quality) and 34" CRT with .5mm pitch @ $700 (near HDTV quality). The cost of the 34" CRT was assumed at around $700 in the RCT.

Projector: The cost of the projection display was obtained by means of a questionnaire. Only one detailed estimate was received from a representative of a major US manufacturer.

5.5 Receiver material cost summary

	MUSE	DigiCipher	DSC-HDTV	CC-DigiCipher	ADTV-HDTV
34" CRT set Electronics only	$258	$188	$219	$227	$216
34" Total	$1048	$978	$1009	$1017	$1006
56" projector Electronics only	$374	$304	$347	$355	$332
56" Proj. Total	$1564	$1494	$1537	$1545	$1522

As can be seen, the average cost of materials for HDTV receivers with 34" CRT is approximately $1011 ± 3% and for 56" HDTV projectors it is $1532 ±3%. This small difference between systems can be considered less than the expected error in the assumptions and underlying data.

6. Receiver Retail Price

Assumptions for high / low product performance and resultant price may be needed to make the cost numbers in this report more useful for market penetration studies. However, the purpose of SG6 was to find the cost of materials and manufacturing of HDTV receivers. It must be understood that selling price is a function of many non-technical factors. Readers of this report who are associated with manufacturers of TV receivers will be able to apply their company's method and philosophy to arrive at a probable selling price.

A very crude estimate of the selling price can be made by multiplying the cost data above by a factor of 2.5. Readers should be advised that SG6 could not agree whether this multiplying factor is accurate or meaningful. This multiplication would result in a 34" HDTV receiver price estimate around $2550. The estimate for a 56" HDTV projector is around $3850.

7. Conclusion

At the outset of this study it was suggested that the cost of the display would have a major impact on HDTV receiver cost. In the course of this study great attention was paid to arrive at realistic cost figures for all receiver components. SG6 attempted to uncover the differences in complexity of the decoders of the proposed systems and to convert these differences into meaningful cost.

The following is a summary of the key results:

- There is a difference between the cost of electronics for the proposed systems but its impact on receiver cost is virtually insignificant. The absolute cost of electronics will decrease rapidly with volume and time, making any cost differential between systems even smaller.
- The cost of the display has a substantial impact on the cost of HDTV and will not reduce appreciably in the near future.
- 34" CRT type HDTV receivers could retail for around $2550.
- 56" HDTV projectors could retail for around $3850.

HDTV Receiver System Comparison Chart

The following table has been assembled from reponses of the proponents. The shaded Functions are for information only and are not part of or included in the receiver cost.

	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
1	Antenna	PS/WP3 SG 2 Use PS/WP3 recommended Antenna	PS/WP3 SG 2 Use PS/WP3 recommended Antenna	PS/WP3 SG 2 Use PS/WP3 recommended Antenna	PS/WP3 SG 2 Use PS/WP3 recommended Antenna	PS/WP3 SG 2 Use PS/WP3 recommended Antenna
2	Tuner type	Double Conv	DCT **Roughly, other proponents' tuner can be used**	Double Conv, 920MHz, 44MHz	DCT **Roughly, other proponents' tuner can be used**	DCT **Roughly, other proponents' tuner can be used**
3	Tuner Presel. Filter	none 1 band VHF 3 band UHF	5 band selectable BP for 2 band VHF, 3 band UHF No tunable filters are needed See final certification materials for details.	Varactor tuned 3-band	5 band selectable BP for 2 band VHF, 3 band UHF No tunable filters are needed See final certification materials for details.	Tuned, 2 BandsVHF, 1 Band UHF
4	Tuner Noise figure	8 dB max	10 dB max	10 dB max	10 dB max	5dB VHF 10dB UHF
5	Tuner LO Number and type	LO1 668-1160 MHz LO2 567 MHz	1st and 2nd LO synthesized from same Xtal to minimize drift problems LO1 1257-2003 MHz LO2 1156.5 MHz	1st LO 4-band synthesizer 0.97 -1.72 GHz 2nd LO = VCO with SAW or ceramic resonator 876 MHz ± 0.3 MHz 3rd LO = FPLL in IF 186.6 MHz + 4	1st and 2nd LO synthesized from same Xtal to minimize drift problems LO1 1257-2003 MHz LO2 1156.5 MHz	LO1 668-1414MHz LO2 567MHz
6	Tuner LO drift	<200 kHz 1st LO <150 kHz 2nd LO	<±50 kHz cumulative Xtal oscillator	<±95kHz cumulative	<±50 kHz cumulative Xtal oscillator	±32kHz covering full step of synthesizer before switching to next step up or down
7	Tuner LO Ph/jitter	<60dB @ fc±10kHz	~95 dBc/Hz @ 10kHz as tested will yield no loss in performance (~75dBc/Hz will result in 0.1dB loss in perf. GI lab test)	~60dB @ fc±1kHz Actual performance as tested is -68dBc/Hz @ ±1kHz	~95 dBc/Hz @ 10kHz as tested will yield no loss in performance (~75dBc/Hz will result in 0.1dB loss in perf. GI lab test)	~95 dBc/Hz @ 10kHz tested (<-75 dBc/Hz @ 10kHz offset. Make up 0.15dB loss in signal to noise by Viterbi decoder. ATRC lab test)

#	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
8	Tuner AFC	± 800 kHz	none used in propotype HDW AFC is provided in the QAM demod. If desired, tuner AFC can be employed. AFC is controlled by the carrier tracking loop. Decision directed carriere tracking loop is used. AFC range is ± 50 kHz	2nd LO = VCO controlled by pilot FPLL in IF	none used in propotype HDW AFC is provided in the QAM demod. If desired, tuner AFC can be employed. AFC is controlled by the carrier tracking loop. Decision directed carriere tracking loop is used. AFC range is ± 50 kHz	µProcessor .... ±3MHz
9	Tuner gain/AGC	25 dB gain 40 dB AGC	60 dB max gain AGC range is 65 dB	Gain 35-40 dB AGC 35-40 dB gain red.	60 dB max gain AGC range is 65 dB	23dB max gain AGC control range 50dB (Gain range -27 - +23dB)
10	Tuner Control & Channel sel.	Electronic tuning	Controlled by µP. Allows channel up/down and direct channel entry. Synthesizer w. 6MHz steps was used in HDW but finer step size can be used for cable & NTSC.	µP controlled, 125kHz step Synthesizer	Controlled by µP. Allows channel up/down and direct channel entry. Synthesizer w. 6MHz steps was used in HDW but finer step size can be used for cable & NTSC.	Synthesized Step size = 32kHz
11	Tuner spec. modes	used for NTSC	used for NTSC	used for NTSC	used for NTSC	Same tuner used for NTSC but different IF
12	IF filter Passband shape	Flat over full 6MHz	SAW -3dB @ 43.5 ± 3MHz was used in tested HDW. center frequency of 44MHz and -3dB @ ±2.65MHz is recommended	SAW Lithium Niobate -3dB @ 44 ± 2.69 MHz	SAW -3dB @ 43.5 ± 3MHz was used in tested HDW. center frequency of 44MHz and -3dB @ ±2.65MHz is recommended	Center frequency 44MHz -1dB @ +2.6MHz/ -3.1MHz?
13	IF filter Stop band att.	>20 dB @ 40.5 / 47.5 MHz >40 dB @ <40.25 / >47.75	-35 dB @ 44 ± 3.0 MHz -50 dB @ 44 ± 3.5 MHz	>- 55dB @ 44 ± 3 MHz NTSC carrier > 63 dB	-35 dB @ 44 ± 3.0 MHz -50 dB @ 44 ± 3.5 MHz	>40dB @ <39.75MHz >40dB @ >47.25MHz >50dB @ 39.75MHz >50dB @ 47.25MHz
14	IF SAW filter spec.	ripple ±1dB Group delay ±50ns	ripple ±.5dB Group delay ± 25 nsec	Transition: ±310kHz Squ Rt Nyquist slopes ripple ±.5dB triple transit < 30 dB Chirp group del. = 1µs	ripple ±.5dB Group delay ± 25 nsec	-1db @ 40.9 and 46.6MHz ±0.25dB Ripple and ±25nsec geoup delay between these points
15	SAW special comments	800 tap	Off the shelf part (not NTSC SAW). SIP 5L package (19mm X 12mm X 5.5mm)	Proto device size 1100 x 250 mils compared to 340 x 86 for NTSC. Cost estimate is $3.50 to $5.00	Off the shelf part (not NTSC SAW). SIP 5L package (19mm X 12mm X 5.5mm)	10mm X 13mm Cost is 6 X NTSC

#	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
16	IF amp. spec.	3 stages, 70 dB overall gain, 40 dB AGC range	3 X 10dB fixed 1 X 0-20dB AGC amp	4 stage amplifier with AGC. 70dB max gain and 65 dB AGC range	3 X 10dB fixed 1 X 0-20dB AGC amp	3 stages 60dB overall gain 50 dB AGC range 2 control stages
17	AGC reference and circuit complexity	Frame pulse during VBI used as reference	IF AGC reference is $I^2 + Q^2$. One bit AGC error output from carrier recovery Symbol synch PROM is integrated by OP Amp and supplied to variable gain amp. 10 dB gain range	Filtered Segment sync used as AGC reference. Block diagram?	IF AGC reference is $I^2 + Q^2$. One bit AGC error output from carrier recovery PROM is integrated by OP Amp and supplied to variable gain amp. 10 dB gain range	IF AGC is referenced to DC Voltage RMS detector is used to compare signal to ref.
18	IF & SAW for NTSC	Same IF can be used for NTSC	Separate NTSC SAW will be used	Separate NTSC SAW will be used	Separate NTSC SAW will be used	Separate NTSC SAW will be used
19	Carrier recovery	Video carrier at 46.8 MHz	Decision Directed Error Detection with 64k X 8 PROM & 512 X 2 PROM. ~±50kHz pull-in for AFC	FPLL to pilot controls 2nd tuner LO 3rd LO @ 4 X IF using SAW res. BW =2kHZ Pull-in ± 100kHz See block diagram in response.	Decision Directed Error Detection with 64k X 8 PROM & 512 X 2 PROM. ~±50kHz pull-in for AFC	Carrier recovery is used as a flag to µP to keep searching or stop 4 MHz crystal reference
20	AFC complexity		2 OP amps & 44MHz VCXO	RCRC LPF for AFC using Q channel output.	2 OP amps & 44MHz VCXO	Same as NTSC
21	IF demod I or I&Q	Synchr. demod for I	Quadrature mixer I & Q	Quadrature mixer I & Q	Quadrature mixer I & Q	Digital synchronous detector operating at 4/T sampling Phase ±1degree Linearity 1%
22	Demod. complexity	Quadrature Mixer	Quadrature Mixer	÷4 counter for 0 and 90°±1° IF carriers.	Quadrature Mixer	2 estimates needed, a)Complexity as tested (to be added) b)Digital proposal see Block diagram
23	Baseband circuits	2 Video amplifiers with 9 MHz band width	2 baseband amps.: Lin = 1%, BW = 10 MHz @ 1dB, GD = ± 10nsec Filter: 2 X 5pole elliptic LPF. Passb.= 5Mhz @ 3dB AC coupled to A/D 10 Hz @ -3dB No clamps used	Baseband limiter Baseband ±1 Multiplier loop integration Filter 8 MHz LPF for I channel, 1 video amp before A/D	2 baseband amps.: Lin = 1%, BW = 10 MHz @ 1dB, GD = ± 10nsec Filter: 2 X 5pole elliptic LPF. Passb.= 5Mhz @ 3dB AC coupled to A/D 10 Hz @ -3dB No clamps used	Baseband done digitally

#	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
24	Modem A/D clock	H-Synch is reference. Regeneration circuit uses LF component	Generated by symbol synch. circuit. Refer to final certification materials.	Derived from symbol synch	Generated by symbol synch. circuit. Refer to final certification materials.	Crystal @ 15.36 MHz / Digital Kostas Loop for clock recovery about 10kHz BW looks at HP and SP channels
25	Modem A/D speed	20 Msps	9.7553 Msps	10.76 Mbps	10.5734 Msps	8bit @ 15.36 MHz
26	Modem A/D number & Spec.	1 X 10 bit	2 X 8bit 6 bit simulated OK	1 X 9 bit linear to 1/2LSB	2 X 8bit 6 bit simulated OK	1 X 8bit Standard Linearity
27	Symbol Synchronization	H sync pulse	Clock Synchr. with 512 X 5 PROM,	75.17 MHz VCXO phase locked to segment sync Symbol clock phase adj. with 2nd 4tap correlator (±1 coeff)	Clock Synchr. with 512 X 5 PROM,	Carrier Recovery Loop related to A/D clock (Divide by 4 & 16) Done part in SW part in HDW. Approx. 10kHz loop filter BW. Complex Multiplier for carrier adjustment
28	Demod circuit complexity	35000 gates 1.3 Mbit RAM 292x ROM (9x12bit) 19.44 MHz				
29	Synchr circuit complexity	One PLL circuit with 0ne Xtal Six 4-bit counters	two + 4 counters, two + 2 counters, one + 1705 counter one + 1050 counter	4 tap matched correlation filter #1 for segment sync.: one 3stage x 9bit SR 3 x 9bit adders 4 tap matched correlation filter #2: one 3stage x 9bit SR 3 x 9bit adders Single tap feedback comb filter: 683 stages, 9 bit wide one 9bit adder 75.32MHz + 7 counter for 10.76 MHz clock. 3 Flip-Flops All other counters operate at 10.76MHz.	two + 4 counters, two + 2 counters, one + 1705 counter one + 1050 counter	2nd order loop 5k gates running at 3 MHz

#	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
30	Frame Synchronization Macro block Synchronization	Frame pulse	A 24-bit sequence is used for frame synch. A 24-bit correlator is used. Macroblock synch. is achieved by using a 16 bit NMP. A 16 bit counter with assoc. random logic is used.	PRNS data frame sync (16.6 ms) add and accumulate segment at a time (2bit signal) PRNS generator 10 bit to 2 bit slicer 2 bit subtractor 2 bit absolute value 10 bit accumulator 10 bit comparator 4 bit confidence counter 2 X 10 bit counters control logic	A 24-bit sequence is used for frame synch. A 24-bit correlator is used. Macroblock synch. is achieved by using a 16 bit NMP. A 16 bit counter with assoc. random logic is used.	1 BYTE at FEC block 8 bit correlator, counter
31	Symbol shaping filter					Option 1: 13800 gates Option 2: 22050 gates
32	Adaptive Equalizer type complex/ real	Real Using training signal	Complex Blind equalization for initial acquisition and decision directed LMS tracking.	Real with PN sequence as reference	Complex Blind equalization for initial acquisition and decision directed LMS tracking.	1FFE: 30 complex taps. 5DFE:complex 5-tap w/50tap delay Alg.: Blind, decision directed LMS algorithm
33	Adaptive Equalizer tap accuracy	Input 10 bit Coefficient 10 bit Output 16 bit	10 bit	10 - 12 bits	10 bit	8bit input, 9bit coefficients 12 bit internal 8bit output
34	Adaptive Equalizer number of taps & complexity	60 tap FIR 300 tap IIR 360 multipliers and adders (42000 gates) 9.72 MHz	FIR 60 complex taps IIR 7 X 4 complex taps 88750 gates	ROM 32 kbits RAM 25 kbits 56900 gates 84 pin PLCC	FIR 60 complex taps IIR 7 X 4 complex taps 88750 gates at 40 MHz.	55 complex mult. 55 adders 2 X 55 delays (holds HP & SP) 300 X 8 bulk delay 5k gates for control and interfacing Option 1: 39940 gates Option 2: 46902 gates
35	Adaptive Equalizer total delay	-2 to +20 µs	-2 to +20 µs	-2 to +20 µs	-2 to +20 µs	-2 to +20 µs
36	Adaptive Equalizer sample rate	9.72 MHz	9.7553 MHz	10.76 MHz	10.5734 MHz	9.6MHz

#	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
37	Adaptive Equalizer Controller	TMS 320	No processor is used.	DSP16A included in equalizer IC	No processor is used.	DSP 56000 or 32030 may use custom if cheaper LMS algorithm RAM 8K x 8 ROM with system µP >70ns access
38	Error correction type	For AUDIO only BCH(82,74) main data BCH(7,3) aux data 25 bit interleaving 1.35 MHz	Trellis Decoder & Reed-Solomon	Reed-Solomon (167,147) t=10	Trellis Decoder & Reed-Solomon	Viterbi decoder, 1/2 code rate zero padded RS code
39	Error correction Constraint length	n.a.	1 TCM encoded bit Trellis Code length 7 (64 states) 4 Soft decision bits Trace-back depth ~ 35 Reed-Solomon for 32QAM (145/155) t=5	Reed-Solomon (167,147) t=10	1 TCM encoded bit Trellis Code length 7 (64 states) 4 Soft decision bits Trace-back depth ~ 35 Reed-Solomon for 32QAM (158/168) t=5	4 bit soft decision, constr. length = 6 RS code type = 148:127, t=8
40	Error correction De-interleaver length	n.a.	Trellis Decoder 32, 8 bit symbols Reed-Solomon Decoder Interleaver length 155bytes X 7?	130 segments x 64µs ea	Trellis Decoder 32, 8 bit symbols Reed-Solomon Decoder Interleaver length 168 bytes X 7	2 deinterleavers, HP & LP 148 bytes ea.
41	Error correction gate count		Trellis decoder: 64 adds, compares & selects per 200 ns 64 X 64 bit path mem 64 X 3 X 4 uncoded bits memory. RS decoder Estimate of 5k gates.	RS decoder 10k CMOS gates 21.5 Mhz rate	Trellis decoder: 64 adds, compares & selects per 200 ns 64 X 64 bit path mem 64 X 3 X 4 uncoded bits memory. RS decoder Estimate of 5k gates.	Dual Viterbi processing: 1 @ 4.8 MHz 1 @ 19.2 Mbps, RS speed 4.8 MHz (8bit)
42	ECC complexity		2 De-interleavers	90k X 4 RAM 8k X 8 ROM 150 flip flops	2 De-interleavers	40 k gates 256 x 8 on-chip RAM for deinterleaving
43	Demux hardware speed		19.5 Mbps 2.44 MHz @ 8bit bytes	21.5 Mbps	21.1 Mbps 2.64 MHz @ 8bit bytes	8 bits @ 3MHz in 12MHz peak out still time muxed to application ICs peak rate @ 12MHz
44	# channels	1 video, 4 audio, 1 128 kbps Data	1 video, 4 audio, 1 126kbps Data, (four 9600 baud + reserve capacity) 1 126kbps Control	1 video 4 audio 1 ancillary data @ 412.9 kb/sec	1 video, 4 audio, 1 126kbps Data, (four 9600 baud + reserve capacity) 1 126kbps Control	assume 4, could be more Video 17.73 Mbps Audio 512 Kbps Data 256 kbps

#	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
45	Decryption method	line rotation & permutation	XOR	XOR	XOR	DES-HW
46	Decryption word length	32 bit key	56 bit key	•	56 bit key	Key = 56 bit Compared in a 64 bit arithmetic
47	Decryption software complexity		15,000 lines of C-code	•	15,000 lines of C-code	
48	Decryption gate count / IC info	600kbits for line permutation, 5kbits for rotation. 6000gates CPU (5MIPS) 9.27 MHz	3,000 gates	•	3,000 gates	8k gates no mem 15k gates for decryption and smart card
49	Pre-decompression buffer memory & type		4 X 1 Mbits	120 bits Xmit Bitmap 1050 bytes for 4 audio channels 861 byte FIFO for aux data 2 X 256k X 4 Compressed Frame buffer 128 kbits MV & coeff	4 X 1 Mbits	32k x 8, >70ns access SRAM Incl on transport IC
50	Buffer mem. rate		2.44 MHz in and 40 MHz out	2.2 MHz in and 40 MHz out	2.64 MHz in and 40 MHz out	>70ns access
51	Image decoder Transform implementation	n.a.	8X8 IDCT	8X8 IDCT / 14bit coeff/ 9bit output. 16bit precision	8X8 IDCT	HP, SP Huffman preprocessing (error modes) MPEG Huffman decoder is @ max 17.73Mbps MPEG IDCT @ 54MHz pixel rate
52	Image decoder LUT		2k X 16 for Huffman 16k X 8 for Inv. Quant.	3 X 16k X 8 ROM	64k X 12 for Huffman 4k X 68 for vector decoding and 16k X 8 for Inv. Quant.	Huffman table ROM t.b.a

#	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
53	Image decoder processing complexity	MUSE	2 estimates: a) 4 Processors of 35,000 gates of logic + 18kbit RAM each b) single more advanced processor (tba)	IC1: Compr. Data FIFO & control, Buffer control, Length decoder, VLC decoder, Inverse quantizer, Scaler, Selection Vector decoder, Motion Vector decoder. estimate 57.5K gates (60 mm^2) 2 X IC2: 1/2 Pel interpolate, Decoding loop arithmetic, Temporal filtering, Block to raster converter, IDCT, U/V chroma upsampling estimate 55K gates (60mm^2)	2 estimates: a) 4 Processors of 35,000 gates of logic + 18kbit RAM each b) single more advanced processor (tba)	Use MPEG information gates: 77k
54	Image decoder circuit speed	mostly 16.2 or 34.4MHz? partially 40 to 48 MHz?	53.6 MHz output speed 13.4 MHz circuit speed	75MHz output speed 37.5 MHz circuit speed	75.5 MHz output speed 15.1 MHz circuit speed	54MHz (some time multiplexing of MPEG decoding operations in RISC architecture 54 MHz pixel rate
55	Image decoder Data width	8bit internal 10bit I/O	8 Bit input 9 bit internal 8 bit output	14 bit IDCT coeff 14 bit motion vectors 8 bit frame buffer 16 bit internal 9 bit IDCT output	8 Bit input 9 bit internal 8 bit output	IDCT 8bit data, 9bit coeff ±256 MV @ 9bits Memory word =64bit Input data =8bits Output bus 28bits
56	Image decoder computation precision	12 bit	12 bits	12 bit internal	12 bits	10 bits
57	Image decoder number of multipliers	45 + 65	•	none - Scaling by table look-up (enties included in LUT ROM) Chroma vertical filtering by shift and add.	•	std IDCT
58	Image decoder number of adders	45 + 65	•	54 additions	•	std IDCT
59	Image decoder RAM size	24.6 Mbits (8bit words)	4 X 350k X 8 Luma 4 X 87.5k X 8 Chroma 4 X 18k X 1 processor	2 X 256k X 16 4 X 256k X 4 min 11.5 Mbits	4 X 60k X 32 Luma 4 X 30k X 32 Chroma 4 X 18k X 1 processor	1frames = 16Mbits 4Mbits of rate buffer + 16Mbits of scratch pad 48Mbits total 3 small 8sample FIFOs

#	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
60	Image decoder RAM config. & type	Standard D-RAM or multiport VRAM	Std RAM can be used but custom RAM will be more economical. Uses multi-port VRAM. Controller included in decoder IC estimate	Standard DRAM	Std RAM can be used but custom RAM will be more economical. Controller included in decoder IC estimate	Std DRAM, no multiport organized as 3 chips (1Mx16b) + 1 chip (256kx16)
61	Image decoder RAM cycle times	30 ns	20 ns	50 ns	10 ns	50 ns
62	Estimated number of production ICs IC size technology	350,000 gates 37Mbit RAM 66x ROM (8x10bit) 48.6 MHz including audio /data excluding equalizer	1 per decoder 140 pins PQFP 35 mm^2 each, 0.7µm CMOS, triple layer metal	2 per decoder 164 pin PQFP 60 mm^2 each 0.5 µm CMOS triple layer metal,	1 per decoder 140 pins PQFP 51 mm^2 each, 0.7µm CMOS, triple layer metal	1 ASIC (probably .5µm in 1996) = memory and std. µC and DSPµC
63	Display clock generator		Part of master VCXO	Part of master VCXO	Part of master VCXO	Separate VCXO derived from MPEG time stamp
64	Decoder RGB post processor	Conversion from YP_bP_r to RGB @ 45 MHz 4000 gates 16 x 11 x 8 ROM	Demux/Filter/ OSD IC for demuxing 4 processors, YUV to RGB, Chroma filters, 15000gates	Used in ATTC test: 6 Tap filter for U/V with 3 mult + 2 add., interpolator LUT 10bit in to 9bit out, LUT for YUV to RGB & gamma	Demux/Filter/ OSD IC for demuxing 4 processors, YUV to RGB, Chroma filters, 15000gates	Analog ?? complexity t.b.a.
65	D/A accuracy and speed	3 X 10bit @ 50 MHz	3 X 8bit (triple) @ 53.6 MHz	3 X 9bit @ 75 MHz	3 X 8bit (triple) @ 75.5 MHz	1 x 8-9bit @ 56MHz 2 x 8-9bit @ 27MHz
66	Post processing filter spec.	sinx/x comp: -3dB @ 18 Mhz -40dB @ 21 MHz Rejection 40dB min	LPF with sinx/x corr., 22MHz @ 3dB. Rejection: -20dB @ 26.5 MHz -40dB @ 31.6 MHz	Sin(x)/x & clock rej. For consumer receiver: use of RLC filter will be sufficient	LPF with sinx/x corr., 31MHz @ 3dB. Rejection: -20dB @ 37.5 MHz -40dB @ 43 MHz	LPF with sinx/x corr., 22MHz @ 3dB. Rejection: -20dB @ 26.5 MHz -40dB @ 31.6 MHz
67	NTSC decoding strategy	Separate decoder can share Tuner and memory	Use low cost std. SAW and NTSC chip. Decoder can share tuner. Memory and A/D could be shared in case of digital decoder.	Use low cost std. SAW and NTSC chip. Decoder can share tuner. Memory and A/D could be shared in case of digital decoder.	Use low cost std. SAW and NTSC chip. Decoder can share tuner. Memory and A/D could be shared in case of digital decoder.	Use low cost std. SAW and NTSC chip. Decoder can share tuner. Memory and A/D could be shared in case of digital decoder.
68	NTSC display processor specs.	NTSC can be upconverted to 1125, 14 tap interpolation filter for line number conversion	525/2:1/29.97 to 1050/2:1/29.97 conversion is needed	525/2:1/29.97 to 787.5/1:1/59.94 conversion is needed (Conv 525/2:1 to 525/1:1 then interpolate 525/1:1 to 787.5/1:1 Horizontal interpolation can be avoided by running D/A converters at lower speed	525/2:1/29.97 to 787.5/1:1/59.94 conversion is needed	same as IDTV Filter ±2dB over passband 8tap interpolating filter for excellent NTSC

#	Function	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T /Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
69	Audio decoding processing complex.	single chip LSI for audio and aux data	16 pin PLCC 17 mm^2, 0.7µm CMOS, triple layer metal	Dolby AC-2 TMS320C53 + D/A + filters	50k gates 2 x D/A 16 pin PLCC 51 mm^2, 0.6µm CMOS,	Yes same cost could be assumed Use MPEG IC Gate count t.b.a.
70	Audio decoding memory requ.	40kbits	4kbit PROM 16kbit RAM	included in TMS320C53	100 kbit PROM 120 kbit RAM	ROM on chip 1Mbit RAM
71	Audio D/A	2 X 16bit 48kHz	incl	2 X 16bit conversion at 47.2 kHz	•	16bit serial PCM @ 48kHz
72	Amplifier and speakers Cost	•Same cost assumption for all systems	Same cost assumption for all systems	Same cost assumption for all systems	Same cost assumption as other systems OK	Same cost assumption for all systems
73	Ancillary Channel processing complex. & capability	included in Audio IC 128 kbps	included in Audio IC with small additional cost		included in Audio IC with small additional cost	500kbps max <200 gates because it is stored in memory and is decoded/used by µC
74	34" CRT specs	1250 x 700	~1400 X 960	1280 X 720 pixels	1280 X 720 pixels	1440 x 960 pixels same CRT can be used
75	Video amplifier spec.	22 MHz	22 MHz at 1Vpp	Video Amp (cost estimated at NTSC X 3)	31 MHz at 1Vpp	22 MHz
76	Deflection system Scan rate	H 33.75 kHz V 60 Hz	H 32 kHz V 59.94 Hz	H 47.2 kHz V 59.94 Hz	H 47.2 kHz V 59.94 Hz	H 32 kHz V 59.94 Hz
77	Deflection component cost		NTSC X 50%	Cost: Yoke NTSC X 1.4 HO-Transistor NTSC X 3 Damper diode NTSC X 3	Display cost estimate at 170% of NTSC cost.	Horizontal output 4X NTSC Yoke = 2X NTSC
78	Power supply specs/cost	400W	<50W for decoder <350W invcl. CRT	Cost: NTSC X 1.1	<50W for decoder <350W invcl. CRT	1.2 x IDTV
79	Cabinet	Same as 16 x 9	Same as 16 x 9		Same as 16 x 9	Same as 16 x 9

HDTV Receiver Cost Table

"#"Numbers are references to functions in the HDTV Receiver System Comparison Chart (RSCC)

	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV(AT&T/Zenith)	CC-DC (ATVA)	AD-HDTV (ATRC)
Tuner cost	$10.00	$13.00	$10.00	$13.00	$13.00
Remarks #2 - #11	Same tuner for NTSC Incl Controller	LO phase jitter tighter spec.Same tuner for NTSC Incl Controller	Same tuner for NTSC Incl Controller	LO phase jitter tighter spec.Same tuner for NTSC Incl Controller	LO phase jitter tighter spec.Same tuner for NTSC Incl Controller
IF SAW filter cost	$3.50				
Remarks #12 - #15	Nyquist shaped filter	Specs and cost ~ same for all digital systems	Specs and cost ~ same for all digital systems	Specs and cost ~ same for all digital systems	Specs and cost ~ same for all digital systems
IF amp. cost	$1	$3.00	$3.00	$3.00	$3.00
Remarks #16	same amp for NTSC	Separate chip set for NTSC	Special design Separate chip set for NTSC	Separate chip set for NTSC	Separate chip set for NTSC
Carrier recovery Demod & AFC/APC & AGC cost	$2.00	$3.40	$0	$3.40	$3.40
Remarks #17, #19 - #22	same for NTSC	64kx8 PROM & 512x2 PROM 2 Op-amps 44MHz VCXO I&Q demod	incl in special IF chip for cable with I&Q demod external RCRC LPF	64kx8 PROM & 512x2 PROM 2 Op-amps 44MHz VCXO I&Q demod	Gates: 16690 incl. A/D & Synch
Analog circuits before A/D	$1	$.50	$.25	$.50	$.70
Remark #23	Same as for NTSC	2 amps + 2 filters	1 amp + 1 filter	2 amps + 2 filters	2 Analog filters
A/D clock circuit cost	$1.50	$0	$0	$0	$1.50
Remarks #24	Same for NTSC	incl in Demod above	Incl. in Sync IC	incl in Demod above	15.32MHz VCXO & Xtal
A/D cost	$10	$0	$0	$0	$0

	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV (AT&T/Zenith)	CC-DigiCipher (ATVA)	AD-HDTV (ATRC)
Remarks #25 & #26	1 x 10bit 20 MHz	2 x 8bit 10 MHz incl in Demod.	1 x 9bit (10bit) 11MHz incl in Equ.	2 x 8bit 11 MHz incl in Demod.	Included in Demod IC
Symbol & Frame Synch. cost	$0	$5.80	$5.10	$10.20	$0
Remarks #27 - #30	n.a.	ROM 4kbit RAM 16kbit Gates: 30k Speed: 27MHz incl. demux & audio/aux	2800 + 1500 gates +7 count at 75MHz all other 11MHz incl. audio & demux	ROM 100kbit RAM 120kbit Gates: 55k Speed: 24MHz incl. demux & audio/aux	Incl in Demod IC
Symbol shaping filter	$9.00	$0	$0	$0	$0
Remarks #31	includes demod	included in Equalizer	included in Equalizer	included in Equalizer	in Demod IC
Adaptive Equalizer cost	$7.00	$7.80	$7.60	$7.80	$5.60
Remarks #32 - #36		ROM 65kbit RAM 5kbit Gates: 90k Speed: 40MHz	ROM 8kx16 SRAM 1kx16 SRAM 1050x9 Gates: 75.2K (350000 Xistors) incl A/D	ROM 65kbit RAM 5kbit Gates: 90k Speed: 40MHz	Gates: Option 2 46902
Adaptive Equalizer Controller	$5.00	$0	$0	$0	$5.00
Remarks #37		incl. in Equalizer	incl. in Equalizer	incl. in Equalizer	DSP 56000 or equ. with RAM 8k x 8
FEC dec. Deinter-leaver cost Viterbi Decoder cost RS decoder cost	$3.00	$3.40	$2.50 + ext DRAM = $2.96 = $5.46	$3.40	$3.30
Remarks #38 - #44	FEC only used for Descrambler & Decryption & Audio	ROM 4kbit RAM 20kbit Gates: 27k Speed: 20Mbps	ROM 8k x 8 RAM 90k x 4 Gates: 10k (150 flip flops) Speed:21.5 Mbps	ROM 4kbit RAM 20kbit Gates: 27k Speed: 20Mbps	25088 bits of mem 35k gates

	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV (AT&T/Zenith)	CC-DigiCipher (ATVA)	AD-HDTV (ATRC)
Image decoder cost (i.e. Muse decoder) or Huffman, IDCT, Motion comp)	$60	$22.00	$27.30(IC1)+ $22.90 (IC2) = $50.20	$42.50	$32.90
Remarks #51 - #58, #62		incl. ROM: 160kbit & RAM: 18kbit Gates: 35k Speed: 54MHz 156 pin	IC1: gates 57.5k incl ROM 384k & RAM 2 x IC2: gates 2 x 55k pad limited/168 pin	incl ROM: 1168 kbit & RAM: 18 kbit Gates: 35k Speed: 75 MHz 156 pin	Gates: 57060 includes some memory
Pre-decomp buffer & Image decoder memory cost	$19.10	$13.37	$9.55	$13.37	$2.50 (SRAM) + $28.65 (DRAM) = $31.15
Remarks #49 -#50, #59 - #61	25 Mbit use 2x16Mbit Includes mem for line number converter	DRAM 16Mbit Hi Speed Data width 32bit (Composed of Y=360Kx32 C=90kx32 Buffer 32kx32 Spare 30kx32)	DRAM 14.5 Mbit RAM 120x1 bitmap RAM 1050x8 FIFO 861x8 RAM 512k x 4 RAM 128k x 1 DRAM 2 x 256 x 16 DRAM 4 x 256 x 4	DRAM 16Mbit Hi Speed Data width 32bit Composed of Y=240Kx32 C=120kx32 Buffer 32kx32 Spare 120kx32	SRAM 32k x 8 DRAM 2 x 1M x 16 DRAM 256k x 16 (48Mbits)
Decoder RGB post processor cost Display Clock Gen	$8.00	$5.40	$5.40	$5.40	$2.90
Remarks #63 - #64	Twice NTSC	ROM 1kbit RAM 1kbit Gates: 15k Speed: 54MHz	ROM	ROM 1kbit RAM 1kbit Gates: 15k Speed: 75MHz	$14mm^2$ bipolar analog IC
D/A cost	$2.00	$2.00	$0	$2.00	$0
Remarks #65		Tripple 8bit D/A Speed: 54MHz	3 x 9bit 75 MHz Incl. in RGB-IC	Tripple 8bit D/A Speed: 75MHz	incl in RGB chip
Analog Post pro-cessing filter	$1.50	$1.50	1.50	$1.50	$1.50

	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV (AT&T/Zenith)	CC-DigiCipher (ATVA)	AD-HDTV (ATRC)
Remarks #66					
NTSC SAW & decoder cost	$8				
NTSC to HDTV display converter cost	$5	$5	$6	$6	$5
Remarks #67 - #68	16kHz - 33kHz	NTSC chip set + 16kHz - 32kHz conv	NTSC chip set + 16kHz - 47kHz	NTSC chip set + 16kHz - 47kHz conv	NTSC chip set + 16kHz - 32kHz conv
Audio & Ancillary decoding cost	$5.00	$0	$0	$0	$5.90
Remarks #69 - #70 #73		Incl in Sync IC	incl. in Sync. IC	Incl in Sync IC	Gates: 45.5k ROM 30k RAM 36k Incl D/A
Audio D/A	$6	$0	$0	$0	$0
Remarks #71	2 x 16 bit 48kHz	Incl in Sync IC	Incl in Sync IC	Incl in Sync IC	16bit serial x 2 @ 48kHz incl. on Audio IC
Signal Processing parts cost	$167.60	$97.67	$115.56	$123.57	$126.35
Amplifier and speakers Cost	$30				
CRT scan system & PS cost Video Amps	$60	$60	$73	$73	$60
Remarks #75 - #78	2 x NTSC Assuming self convergence	2 x NTSC Assuming self convergence	3 x NTSC Assuming self convergence and availability of suitable components	3 x NTSC Assuming self convergence and availability of suitable components	2 x NTSC Assuming self convergence
Total circuit parts cost	$257.60	$187.67	218.56	226.57	$216.35
34W CRT cost	$700				

	MUSE (NHK)	DigiCipher (ATVA)	DSC-HDTV (AT&T/Zenith)	CC-DigiCipher (ATVA)	AD-HDTV (ATRC)
Remarks #74	NTSC 35V with 0.7mm dot pitch = $550 now. In 1996 34W Invar with 0.7mm dot pitch ~ $550 34W for near HDTV with ~ 0.5mm - 0.6mm ~ $700. No cheaper alternate technology 34W for full HDTV with ~ 0.3mm - 0.4mm ~ $1000. anticipated for this size and performance				
CRT cabinet cost #79	$90.00				
34W instrument parts cost	$1047.60	$977.67	$1008.56	$1016.57	$1006.35
Projector scan /conv system & PS cost, Video Amps	$176	$176	$201	$201	$176
Remarks Alternate to #75-#78					
Total Projector circuit parts cost	$373.60	$303.67	$346.56	$354.57	$332.35
56W Proj. Screen, Optics, CRTs & assembly Alternate to #74	$1050				
Projector cabinet cost Alt #79	$140				
Total cost for 56W receiver	$1563.60	$1493.67	$1536.56	$1544.57	$1522.35