ERICSSON

May 25, 2016

Ex Parte

Marlene H. Dortch
Secretary
Federal Communications Commission
445 12th Street SW
Washington, DC 20554

RE: Use of Spectrum Bands Above 24 GHz for Mobile Radio Services, et al., GN Docket No. 14–177, RM–11664

Dear Ms. Dortch:

On May 23, 2016, Anders Svensson, Kumar Balachandran, Farshid Ghasemzadeh, Mark Racek, Sanjay Dhawan and Vladimir Bazhanov of Ericsson, met with Michael Ha, Bahman Badipour, Rashmi Doshi, Reza Biazaran of the Federal Communications Commission's ("Commission") Office of Engineering and Technology and Chris Helzer of the Wireless Telecommunications Bureau to discuss the above-captioned proceeding.

Ericsson discussed using Total Radiated Power ("TRP") as the proper metric for measuring unwanted emissions for advanced antenna array systems. TRP requires that the sum of all emissions from all transceivers in the advanced antenna array should be kept below the required unwanted emission level, and in practice the level of unwanted emissions per transceiver in the antenna array would need to be kept 10·log10(n) dB lower (where n is the number of transceivers) than the required unwanted emission level which is also fully in line with FCC's MIMO/Multiple transmitter requirements. However, Ericsson would also support the option of using "conducted equivalent" measurements, which is similar to TRP as both metrics correspond to same unwanted emission requirement.

Ericsson also discussed raising the proposed power limits. The Notice of Proposed Rulemaking proposed power limits of 62 dBm EIRP measured over 100 MHz. Power is the most challenging and costly resource in mobile communications, and there is no incentive to utilize more than what is necessary. Therefore Ericsson urges the Commission to give equipment manufacturers and network operators greater flexibility to manage power and engineer innovative technical improvements, in lieu of an overly restrictive ceiling.

For millimeter wave bands, beam forming is made possible with massive array antennas. With small wavelengths, element separation is greatly reduced to the order of millimeters and it is therefore possible that radios may be built with as many as 512 elements (e.g., 16x16, cross-polarized), each with an integrated Power Amplifier ("PA") within a small total footprint. The combination of these PAs and antenna elements can by themselves achieve

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transmission power levels above the Commission's proposed 62 dBm/100 MHz level. If these antenna elements can be driven by Gallium Nitride ("GaN") PAs, even more gains in power levels can be achieved as long as the thermal effects can be managed.

The power capability of power amplifiers for integrated circuit technology is improving over time and in particular GaN integrated circuit PA technologies are evolving rapidly and deliver power levels an order of magnitude higher compared to conventional technologies such as CMOS as shown in the figure below. Thus, a transition to GaN PA technology together with efficiency improvement schemes would pave the way for higher achievable EIRP for millimeter-wave systems. In addition to possible EIRP increases due to improvement in PA integrated circuit technology power capability such as GaN, increasing the number of sub-arrays (transceiver and corresponding radiating elements) could also result in increased EIRP.

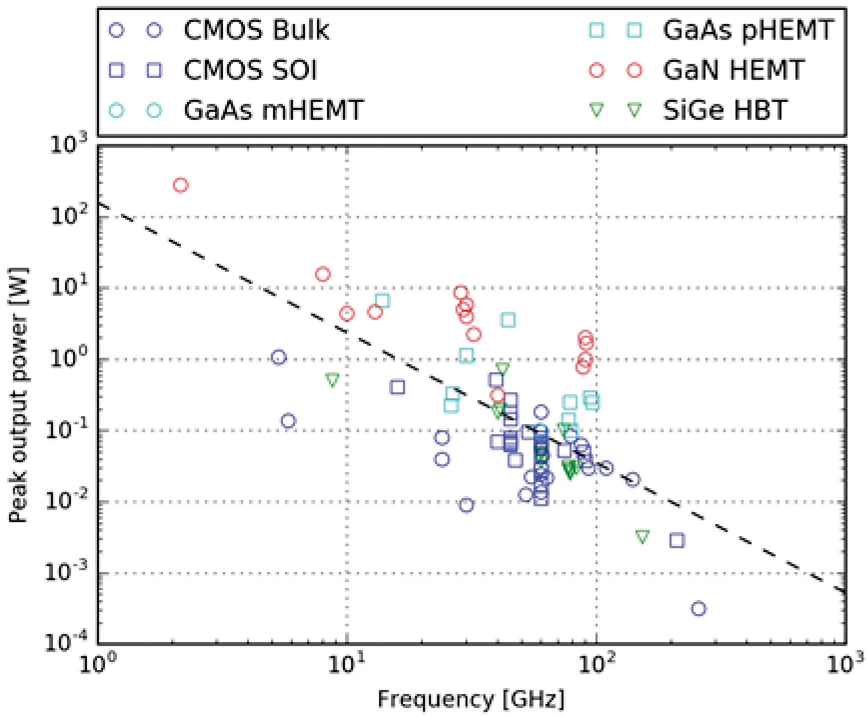


Figure 1. **Power amplifier output power versus frequency for various semiconductor technologies. The data points are taken from an internal Ericsson survey or published microwave and mm-wave power amplifier circuits.**

Additional details can be found in the attached Ericsson submission to 3GPP titled *On mm-wave technologies for NR.*

Sincerely,

/s/ Mark Racek
Mark Racek
Sr. Director, Spectrum Policy

Attachment

cc: Julius Knapp
Jon Wilkins
Michael Ha
Bahman Badipour
Rashmi Doshi
Reza Biazaran
Chris Helzer

ATTACHMENT

3GPP TSG-RAN WG4 #79 **Tdoc R4-164226**
Nanjing, China, 23rd – 27th May 2016

Source: **Ericsson**
Title: **On mm-wave technologies for NR**
Agenda Item: **9.4**
Document for: **Discussion**

1 Introduction

The objective of New Radio (NR) SI is not only to develop requirements and specifications for NR access technology (up to 100 GHz) but also provide sharing parameters for frequency band within 24 GHz to 86 GHz as requested in an LS from ITU-R WP5D. Work plan for the ITU-R related work were discussed in previous RAN4 meeting. Early start of the mm-wave work in RAN4 is thus essential for development of requirements for NR as well as handling the ITU-R related work.

In this paper, we initiate the discussion on some important and fundamental aspects related to mm-wave technologies to better understand the performance that mm-wave technology can offer but also the limitations.

Areas such as AD/DA converters, power amplifiers and the achievable power versus efficiency as well as linearity are further discussed. In addition, we provide some detailed insight into the receiver essential metrics such as noise figure, bandwidth, dynamic range, power dissipation and the dependencies. The mechanism for frequency generation as well as phase noise aspects is also covered in this paper. The filters for mm-waves is another important part of this paper indicating the achievable performance for various technologies and the feasibility of integrating such filters into NR implementations.

To reach common understanding is an important step to be able to create proper requirement for mm-wave frequencies.

2 Discussion

The 3GPP work and existing specifications from 2G and beyond are considering frequency ranges below 6 GHz and the technology aspects related to this particular frequency range. No work on frequencies above 6 GHz for any 3GPP specifications has been conducted up to now and so given the objective of covering frequency ranges up to 100 GHz for NR, it is essential to discuss the mm-wave specific technology aspects. In this paper, an overview of some important and fundamental mm-wave aspects is provided. We will further elaborate and discuss in detail the relevant aspects during the coming meetings where more time units are available for NR work and encourage other companies to contribute in this area.

The intention is to initiate the discussion without considering any restrictions nor proposing specific models or mandating any implementation, but rather highlight the possibilities for mm-wave receiver and transmitters to align and come to a common understanding. It is quite essential to consider all of these aspects of mm-wave technology before any core requirements are settled. In addition, the LS response to ITU-R, beside the needed co-existence study should also consider the achievable technology potential to make sure that the input parameters to ITU-R studies are not only relevant but also close what the future 3GPP standard would specify.

The data used in this paper for various aspects is either published elsewhere or is based on internal measurements indicating the current state-of-the-art capability and performance.

The compact building practice needed for mm-wave systems with many transceivers and antennas requires careful and often complex consideration regarding the power efficiency and heat dissipation in small area/volume. These considerations directly affect the achievable performance and possible 3GPP requirements. The discussion in this paper in many aspects not only applies for NR BS but also NR UE as the mm-wave transceiver implementation between UE and BS would differ less compared to frequency bands below 6 GHz.

2.1 ADC and DAC considerations

The larger bandwidths available at mm-wave communication will challenge the data conversion interfaces between analog and digital domains in both receivers and transmitters. The Schreier Figure-of-Merit (FoM) is a widely accepted metric for ADC defined by $FoM_{schreier}=DR+10log10(BW/P_{DC})$ with Dynamic Range (DR) in dB, power consumption PDC in W, and signal bandwidth BW in Hz. Figure 1 shows the Schreier FoM for a large number of published ADCs [Murmann15] vs. the Nyquist sampling frequency f_{snyq} (=2xBW for most converters). The dashed line indicates the $FoM_{schreier}$ envelope which is constant at roughly 170dB for sampling frequencies below some 100MHz.

With constant FoM the power consumption doubles for every doubling of bandwidth or 3dB increase in DR. Above 100MHz there is an additional 10dB/decade penalty and this means that a doubling of bandwidth will increase power consumption by a factor of 4.

Although the FoM envelope is expected to be slowly pushed toward higher frequencies by continued development of integrated circuit technology, RF bandwidths in the GHz range inevitably give poor power efficiency in the analog-to-digital conversion.

Thus, the large bandwidths and array sizes assumed for NR at mm-wave will inevitably lead to a large ADC power footprint and it is extremely important that specifications driving dynamic range requirements are not unnecessarily high. This applies to UEs as well as BS.

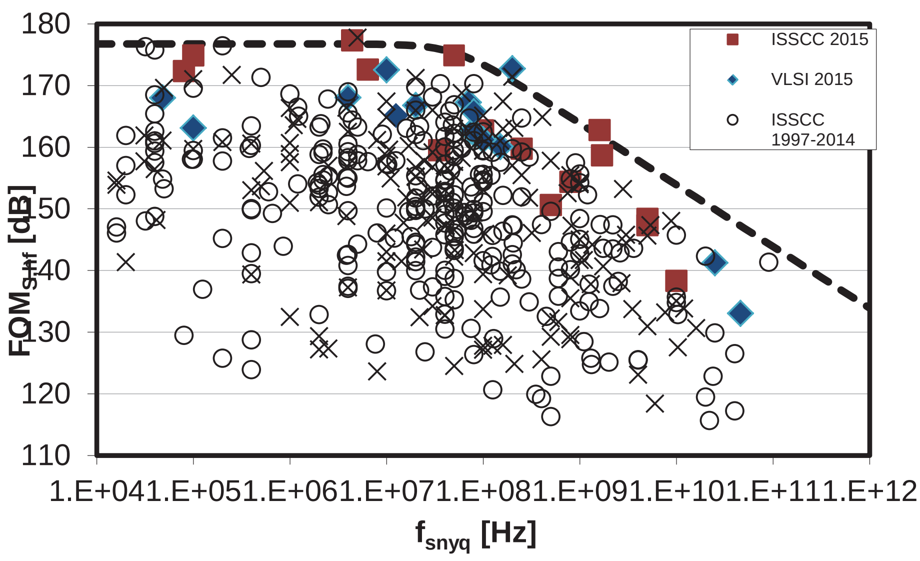


Figure 1 Schreier figure-of-merit for published ADCs.

Digital-to-analog converters (DAC) are typically less complex than their ADC counterparts for the same resolution and speed. Furthermore, while ADC operation commonly involves iterative processes, the DACs do not. DACs do also attract substantially less interest in the research community. While structurally quite different from their ADCs counterparts they can still be benchmarked using the same FoM and then render similar numbers as for ADCs. Thus, similar to an ADC, a larger bandwidth and unnecessarily high dynamic range requirement on the transmitter would also result in higher DAC power foot print and need to be considered.

2.2 Lo generation and Phase noise aspects

All modern communication systems apply a Local Oscillator (LO) to shift carrier frequency up- or down-wards in their transceivers. A critical LO feature is the so-called Phase Noise (PN) of the signal generated by the LO. In plain words phase noise is a measure of how stable the signal is in the frequency domain. Its value in dBc/Hz at a given offset frequency Δf describes how likely the signal frequency deviates by Δf from the desired frequency, f_0.

LO phase noise may significantly impact system performance; this is illustrated, though somewhat exaggerated, by figure 2 where the constellation diagram for a 16-QAM signal is compared for cases with and without phase noise. Therefore, for a given level of symbol error rate, phase noise limits the highest modulation scheme that may be utilized. In other words, different modulation schemes pose different requirements on the LO phase noise level.

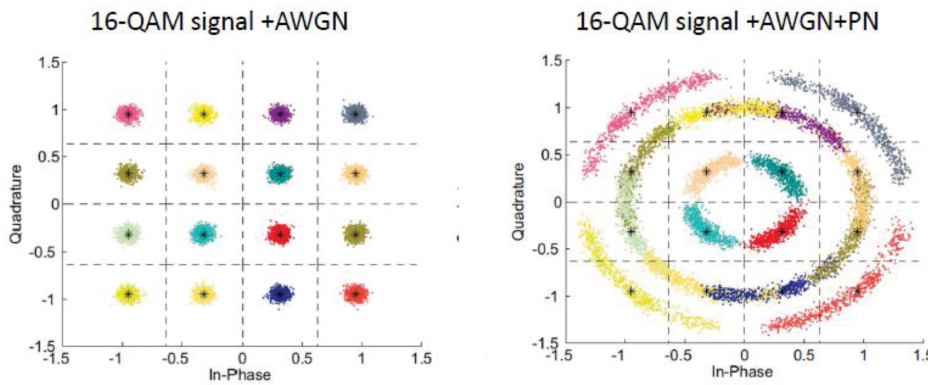
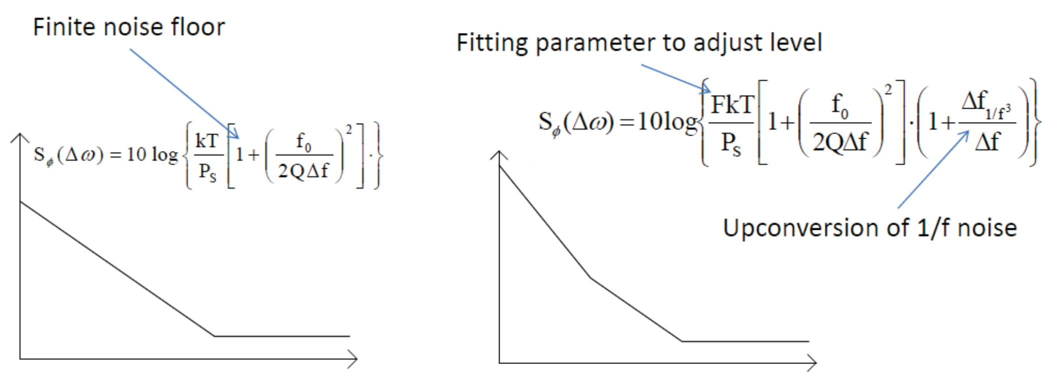


Figure 2, Constellation diagram of a 16-QAM signal without (left) and with (right) phase noise.

2.2.1 Phase noise characteristics of free-running oscillators and PLLs

The most common circuit solution for frequency generation is to use a Voltage Controlled Oscillator (VCO). The phase noise of a typical VCO can be described by, for example, the Leeson equation shown below, or various Figure of Merit equations. Figure 3 shows the model and the typical behavior of a free-running VCO in different regions of operation, where f_0 is the oscillation frequency, Δf is the offset frequency, P_s is the signal strength, Q is the loaded quality factor of the resonator, F is an empirical fitting parameter but has physical meaning of noise figure, and $\Delta f_{1/f^3}$ is the 1/f-noise corner frequency of the active device in use.



**Leeson DB, "A Simple model of feedback oscillator noise spectrum, Proc. IEEE 54(2), 329-330, 1966

Figure 3 Phase noise characteristic for a typical free-running VCO according to Leeson: without 1/f noise (left) and with 1/f noise (right)

Based on the Leeson equation, some conclusions may be drawn which will be discussed further when challenges with generating mm-wave frequencies are dealt with:

1. PN increases by 6 dB every time when f_0 doubles
2. PN is inversely proportional to signal strength, P_s
3. PN is inversely proportional to the square of the loaded quality factor of the resonator, Q
4. 1/f noise up-conversion gives rise to close-to-carrier PN increase (small offset)

Therefore, there are several design parameters that may be used as tradeoffs in VCO development. Commonly, the VCO performance is well captured through a Figure-of-Merit (FoM) defined by the equation below, taking into account power consumption and allowing for a comparison of different VCO implementations (in terms of semiconductor technology, circuitry topology, etc.):

$$FoM = PN_{VCO}(\Delta f) - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log(P_{DC}/1mW)$$

Here $PN_{VCO}(\Delta f)$ is the phase noise of the VCO in dBc/Hz at a frequency offset Δf with oscillation frequency f_o (both in Hz) and power consumption P_{DC} in W. One noticeable result of this expression is that both phase noise and power consumption in linear power are proportional to f_0^2. Thus, to maintain a phase noise level at a certain offset while increasing f_o by a factor R would require the power to be increased by R^2 (assuming a fixed FoM). Conversely, for a fixed power consumption and FoM the phase noise will increase by R^2, or 6dB per every doubling of f_0.

A common way to suppress the phase noise is to apply a Phase Locked Loop (PLL), as shown in figure 4. The basic building block is a VCO which is locked to a highly stability reference (normally a low frequency XO).

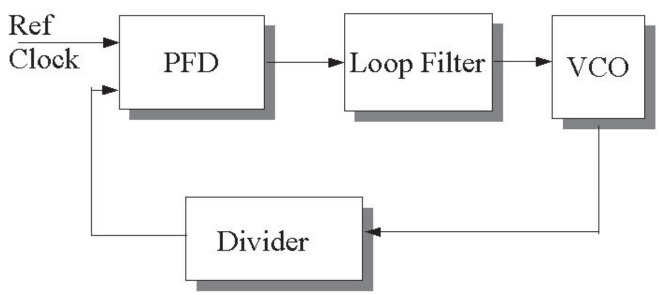


Figure 4 block diagram of a Phase Locked Loop (PLL)

The total phase noise of the PLL output is composed of contributions from the VCO outside the loop bandwidth and the reference oscillator inside the loop. A significant noise contribution is also added by the phase detector and the divider. Figure 5 shows the typical behavior of the PLL phase noise in different offset frequency regions. As a matter of fact, it is the measured phase noise from a ~28 GHz LO (by applying a PLL at a lower frequency and then multiplied to ~28 GHz). Obviously, there are four different offset ranges that show distinctive characteristic:

1. f_1, for small offsets, <100kHz: ~ -30dB/decade roll-off, contributed by 1/f noise up-conversion
2. f_2, for offsets within the PLL bandwidth: relatively flat, composed of several contributions
3. f_3, for offsets larger than PLL bandwidth: -20dB/decade roll-off, dominant by VCO phase noise
4. f_4, for even large offset, >10 MHz: flat, due to finite noise floor

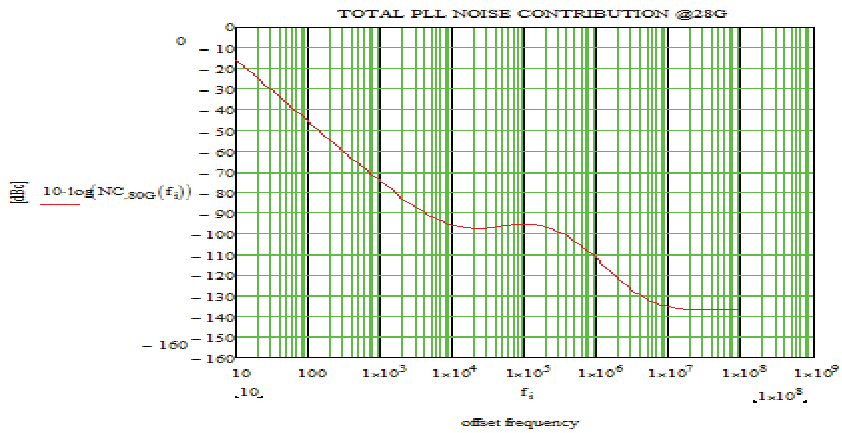


Figure 5 Example of measured phase noise behavior for a phase locked VCO multiplied to ~28 GHz

2.2.2 Challenges with mm-Wave frequency generation

As phase noise increases by 6dB per doubling of the frequency, it would never be expected that a mm-wave LO exhibits comparable PN performance compared to a lower frequency LO. Moving up oscillation frequency from 3 GHz to 30 GHz, for instance, will fundamentally result in PN degradation of 20 dB for a given offset frequency. This will certainly limit the highest usable order of the PN-sensitive modulation schemes at mm-wave, and thus poses limitation on achievable spectrum efficiency for mm-wave communication systems.

Additionally, a PN increase at mm-wave is also caused by the degradation in quality factor Q and the signal power P_s. Leeson's equation tells us that in order to achieve low phase noise Q and P_s need to be maximized while minimizing the noise figure of the active device. Unfortunately, all these three factors contribute in an unfavorable manner when oscillation frequency increases. In monolithic VCO implementation, the Q-value of the on-chip resonator decreases rapidly as frequency increases due mainly to (i) the increase of parasitic losses such as metal loss and/or substrate loss and (ii) the decrease of varactor Q. Meanwhile, the signal strength of the oscillator becomes increasingly limited when going to higher frequencies. This is because higher frequency operation requires more advanced semiconductor devices whose breakdown decreases as its feature size shrinks. For this reason, a typical way of generating mm-wave signals ranging from 6 to 100 GHz is to have the fundamental VCO frequency at some 5 to 15 GHz and use frequency multipliers to reach the wanted final frequency.

Except for the challenges discussed so far, up-conversion of the 1/f noise creates an added slope close to carrier. The 1/f noise is heavily technology dependent where planar devices such as FET, PHEMT and CMOS are showing a higher noise than vertical bipolar devices like Si bipolar, SiGe HBT and GaAs HBTs. Figure 6 summarizes phase noise performance vs oscillation frequency for different semiconductor technologies.

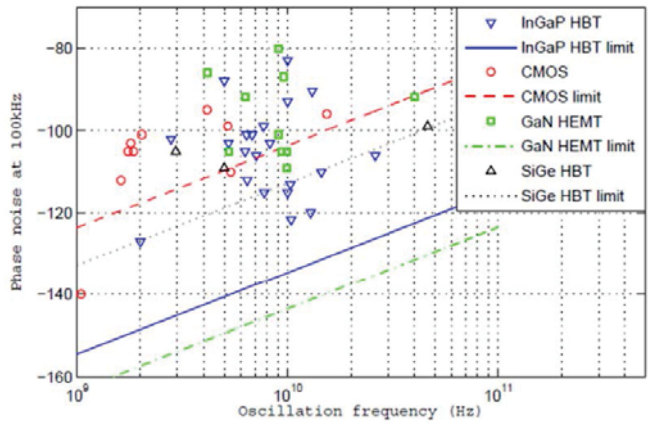


Figure 6 Phase noise performance for different technologies [ref?]

For reasonable cost and size efficiency a fully integrated MMIC/RFIC VCO solution is preferred and depending on technology the full PLL system can be included. Technologies used are ranging from CMOS and BiCMOS to III-V materials where InGaP HBT is popular due to reasonable low 1/f noise and high breakdown but occasionally also PHEMT devices are used even if suffering from severe 1/f noise. Some development has been made using GaN FET structures in order to benefit from the very high breakdown voltage but 1/f is even higher than in GaAs FET devices and therefore seems to offset the gain of the breakdown voltage.

We will further elaborate on frequency generation and phase noise in the coming meetings.

2.3 PA efficiency in relation to unwanted emission

Radio Frequency (RF) building block performance generally degrades with increasing frequency. The power capability of power amplifiers for a given integrated circuit technology roughly degrades by 20 dB per decade, as shown in Figure 7. There is a fundamental cause for this degradation; increased power capability and increased frequency capability are conflicting requirements as observed from the so-called Johnson limit. In short, higher operational frequencies require smaller geometries, which subsequently result in lower operational power in order to prevent dielectric breakdown from the increased field strengths. Moore's Law does not favor power capability performance.

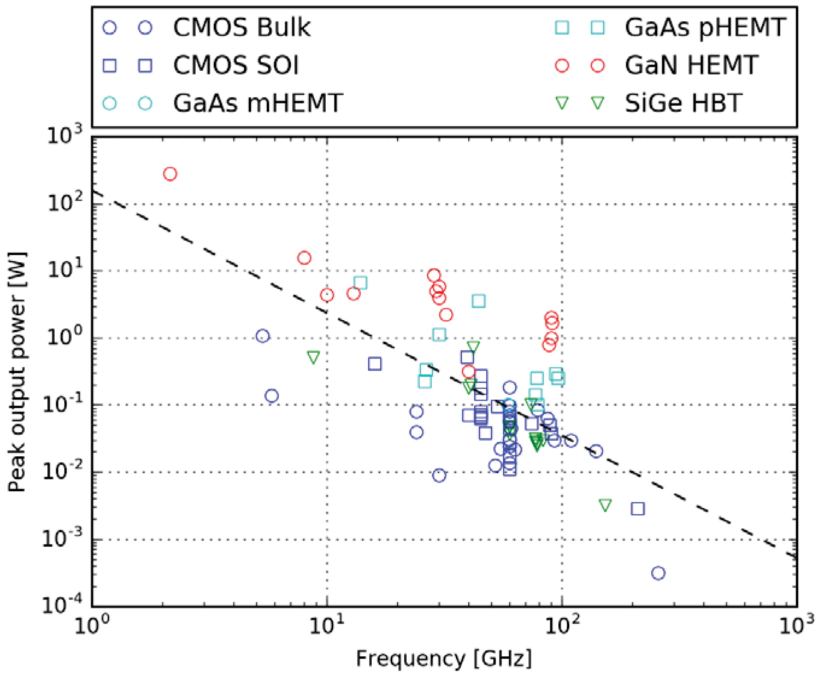


Figure 7 Power amplifier output power versus frequency for various semiconductor technologies. The dashed line illustrates the observed reduction in power capability versus frequency (-20 dB per decade). The data points are taken from an internal Ericsson survey of published microwave and mm-wave power amplifier circuits.

A remedy is however found in the choice of integrated circuit material. Mm-wave integrated circuits have traditionally been manufactured using so called III-V materials, i.e. a combination of elements from groups III and V of the periodic table, such as Gallium Arsenide (GaAs) and more recently Gallium Nitride (GaN). Integrated circuit technologies based on III-V materials are substantially more expensive than conventional silicon-based technologies and they cannot handle the integration complexity of e.g. digital circuits or radio modems for cellular handsets. Nevertheless, GaN-based technologies are now maturing rapidly and deliver power levels an order of magnitude higher compared to conventional technologies.

There are mainly three semiconductor material parameters that affect the efficiency of an amplifier: the maximum operating voltage, maximum operating current density and knee-voltage. Due to the knee-voltage, the maximum attainable efficiency is reduced by a factor proportional to:

$$\frac{1-k}{1+k}$$

Where *k* is the knee-voltage to the maximum operating voltage ratio. For most transistor technologies the ratio *k* is in the range of 0.05 to 0.01, resulting in an efficiency degradation of 10% to 20%.

The maximum operating voltage and current density limits the maximum output power from a single transistor cell. To further increase the output power, the output from multiple transistor cells must be combined. The most common combination techniques are stacking (voltage combining), paralleling (current combining), and corporate combiners (power combining). Either choice of combination technique will be associated with a combiner-efficiency. A lower power density requires more combination stages and will incur a lower overall combiner-efficiency. At mm-wave frequencies the voltage- and current-combining methods are limited due to the wave-length. The overall size of the transistor cell must be kept less than about 10th of wavelength. Hence, paralleling and/or stacking are used to some extent and then corporate combining is used to get the wanted output power. The maximum power density of CMOS is about 100 mW/mm compared to 4000 mW/mm for GaN. Thus GaN technology will require less aggressive combining strategies and hence higher efficiency.

Figure 8 shows the saturated power added efficiency (PAE) as function of frequency. The maximum reported PAE is about 40% and 25% at 30 GHz and 77 GHz, respectively.

PAE is expressed as PAE = 100*{$[P_{OUT}]_{RF} – [P_{IN}]_{RF}$} / $[P_{DC}]_{TOTAL}$.

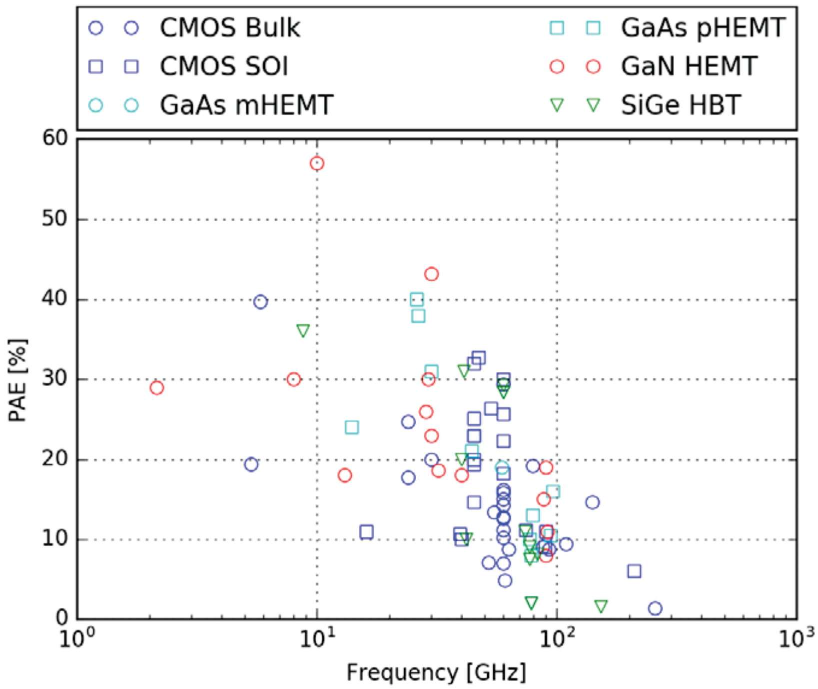


Figure 8 Saturated power added efficiency versus frequency for various semiconductor technologies. The data points are taken from an internal Ericsson survey of published microwave and mm-wave power amplifier circuits.

At mm-wave frequencies the available output power is fundamentally limited by semiconductor technologies. Furthermore, the efficiency is also degraded with frequency.

Considering the PAE characteristics in figure 8, and the non-linear behavior of the AM-AM/AM-PM characteristics of the power amplifier, significant power back-off would be necessary to reach certain linearity requirement such as ACLR. Considering the heat dissipation aspects and significantly reduced area/volume for mm-wave products, the complex interrelation between linearity, PAE and output power in the light of heat dissipation should be considered. We will further elaborate on this in the coming meetings.

2.4 Filtering aspects

Various types of filters have been deployed in 3GPP based BS and UE implementations below 6 GHz. The filters mitigated the unwanted emissions arising from e.g. non-linearity in the transmitters generated due to intermodulation, harmonics generation etc. In the receiver chain filters where deployed to handle either own transmitter in paired bands or suppress the interferer at adjacent or other frequencies.

The requirements have also been differentiated in terms of levels e.g. for spurious emission, general, co-existence in the same geographical areas and co-location has been specified while the requirement levels for in-band to out-of-band has also been considered by exclusion zones defining e.g. the in-band and spurious emission domain respectively.

For mm-wave frequencies depending on the waveform design and OFDM numerology, different modulation spectrums affecting the filtering and size of the exclusion zones should be considered. The modulation spectrum aspect is further discussed in [1].

Considering the limited size (area/volume) and level of integrations needed for mm-wave frequencies, the filtering can be challenging where discrete mm-wave filters are far too bulky to be fitted in limited size as well as the challenge it poses to embed such filter into highly integrated structures for mm-wave products.

2.4.1 Possibilities of filtering in the analogue front-end

Different implementations provide different possibilities for filtering. For the purpose of discussion we distinguish between two main cases:

- Low-cost, monolithic integration with one or a few multi-chain CMOS/BiCMOS core-chip with built-in power amplifiers and built in down-converters. This case will give limited possibilities to include high performance filters along the RF-chains since the Q-values in on chip filter resonators will be poor (5-20).
- High performance, heterogeneous integration with several CMOS/BiCMOS core chips, combined with external amplifiers and external mixers. This implementation allows the inclusion of external filters along the RF-chains (at a higher complexity, size, and power consumption).

There are at least three places where it makes sense to put filters, depending on implementation:

- Behind or inside the antenna element (F1 or F0), where loss, size, cost and wide-band suppression is important.
- Behind the first amplifiers (looking from the antenna side), where low loss is less critical (F2).
- On the high frequency side of mixers (F3), where signals have been combined (in the case of analogue and hybrid beam forming).

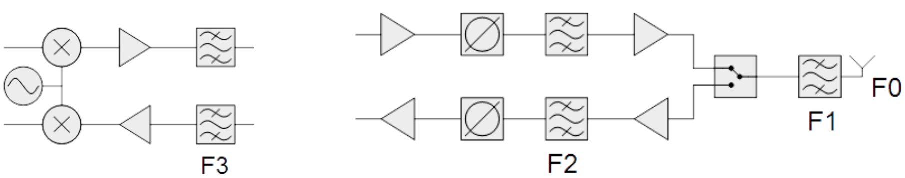


Figure 9 Possible filter placements

The main purpose of F1/F0 is to suppress interference and emissions far from the desired channel across a wide frequency range (e.g. DC-60 GHz). There should not be any un-intentional resonances or passbands in this wide frequency range. This filter will help relax the design challenge (bandwidth to consider in optimizations, and linearity requirements) of all following blocks. Insertion loss must be very low, and there is a strict size and cost requirements since there possibly will be one filter at each sub-array.

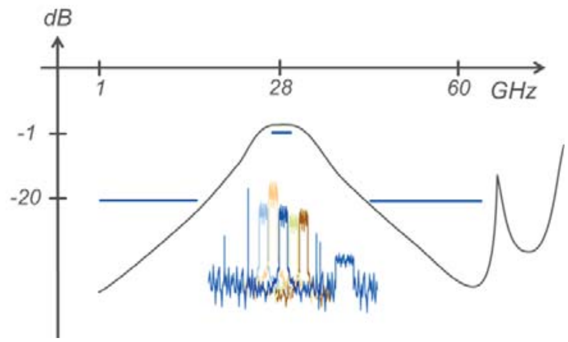


Figure 10 Filter example

The main purpose of F2 would be to suppress LO leakage and unwanted mixing products, and it will also add image rejection and rejection of general interference a few channels away from the carrier. There are still strict size requirements, but more loss can be accepted (behind the amplifiers) and also un-intentional passbands (since F1/F0 will handle that). This enables better frequency precision (half-wave resonators) and better discrimination (more poles).

The main purpose of F3 would be to suppress LO leakage and unwanted mixing products, but there is also a possibility to obtain suppression in neighbouring channels, to protect mixer and ADC. For analogue (or hybrid) beam-forming it is enough to have just one (or a few) such filter(s). This relaxes requirements on size and cost, which opens the possibility to achieve high Q and high precision.

The deeper in the RF-chain the filtering is placed (starting from the antenna element) the better protected the circuits will get.

For the monolithic integration case it is difficult to implement filters F2 and F3. One can expect performance penalties for this case. In addition, output power is typically lower.

In addition, the shielding to achieve isolation over high frequency range can be challenging, as microwaves have a tendency to bypass filters by propagating in ground structures around them.

2.4.2 Insertion loss (IL) and bandwidth

Sharp filtering on each branch (at positions F1/F0) with narrow bandwidth leads to excessive loss at microwave and mm-wave frequencies. To get the insertion loss down to a reasonable level one the passband can be made significantly larger than the signal bandwidth. A drawback of such an approach is that several unwanted neighbouring wideband channels will pass the filter. In choosing the best loss-bandwidth trade-off there are some basic dependencies to be aware of:

- IL decreases with increasing BW (for fixed fc).
- IL increases with increasing fc (for fixed BW).
- IL decreases with increasing Q.
- IL increases with increasing N.

To exemplify the trade-off we study a 3-pole LC-filter with Q=20, 100, 500 and 5000, for 100 and 800 MHz 3dB-bandwidth, tuned to 15 dB equal ripple (with Q=5000) is examined in Figure 11.

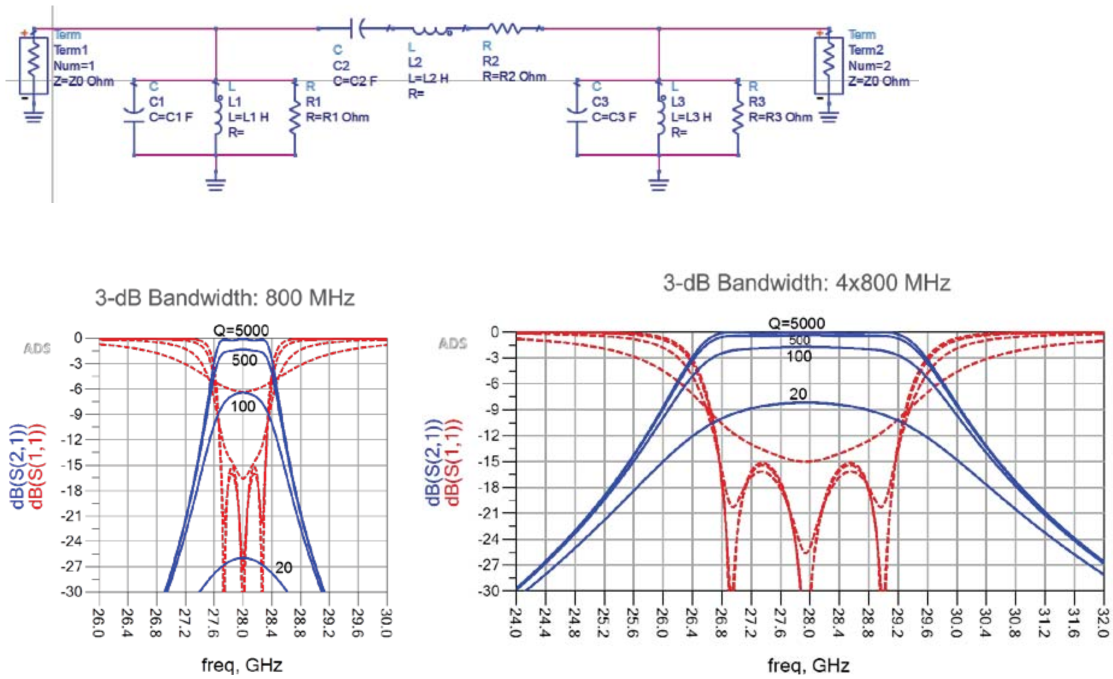


Figure 11 Example 3-pole LC filter with 800 and 4x800 MHz bandwidth, for different Q value

From this study we observe:

- 800 MHz bandwidth or smaller, requires exotic filter technologies, with a Q-value around 500 or better to get an IL below 1.5 dB. Such Q-values are very challenging to achieve considering constraints on size and cost.
- By relaxing the requirement on selectivity to 4x800 MHz, it is sufficient to have a Q-value around 100 to get 2 dB IL. This should be within reach with a low-loss, PCB. The margin in terms of bandwidth will help to accommodate typical production tolerances of the PCB.

2.4.3 Filter implementation examples

In principle, there are many ways to implement filters in a 5G array radio. Key aspects to compare are: Q-value, discrimination, size and integration possibilities. The following table gives a rough comparison between different technologies.

Technology	Q	Size	Integration
On-chip (Si)	20	Small	Feasible
PCB (low-loss)	100	Medium	Feasible
Thin film (ceramic)	300	Medium	Difficult
MEMS/Advanced miniature filters	500	Medium	Difficult
Waveguide	5000	Large	Extremely difficult

An attractive way to implement the antenna filter (F1) is to use a strip-line or micro-strip filter, embedded in a PCB close to each antenna element. This requires a low loss PCB with good precision. Production tolerances (patterning and via-positioning) will limit the performance, mainly though a shift in the pass-band and increased mismatch. In most implementations the passband must be set larger than the operating frequency band with significant margin to, account for this.

A 2-pole example of such a filter is shown in the figure below, along with simulation results (valid for a strip-line embedded in 500 um dielectric with ε=3, tanδ=0.013, with metal roughness ignored). Typical characteristics are:

- Centre frequency: 28 GHz
- 3 dB bandwidth: 4x800 MHz
- Insertion loss: 0.6 dB (which could double due to roughness).
- Stopband 1: -30 dB within DC-21 GHz
- Stopband 2: -30 dB within 38-68 GHz
- Size 2x5 mm (substrate size in the figure)

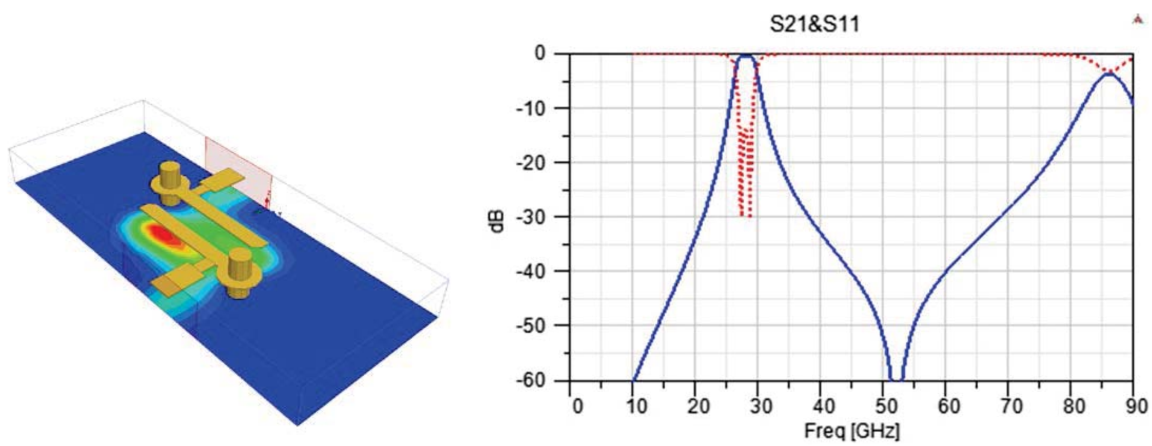


Figure 12 Example of strip-line mm-wave filter

As seen in the plot, this state-of-the-art mm-wave implementation of the outermost filter (F1) will give fairly high attenuation across large frequency ranges, but we cannot expect any attenuation in the nearest few neighbouring wideband channels. In this example there is a higher order passband around 90 GHz, which can potentially be suppressed by the addition of low-pass or band-stop sections.

We will further elaborate on these aspects in the coming meetings.

2.5 Noise figure, dynamic range and bandwidth dependencies

The dynamic range (DR) of a cellular receiver will in general be limited by the front-end insertion loss (IL), the receiver (RX) LNA and the ADC noise and linearity properties.

Typically $DR_{LNA} \gg DR_{ADC}$ so the RX use AGC and selectivity (distributed) in-between the LNA and the ADC to optimize the mapping of the wanted signal and the interference to the DR_{ADC}. For simplicity we only consider a fixed gain setting here.

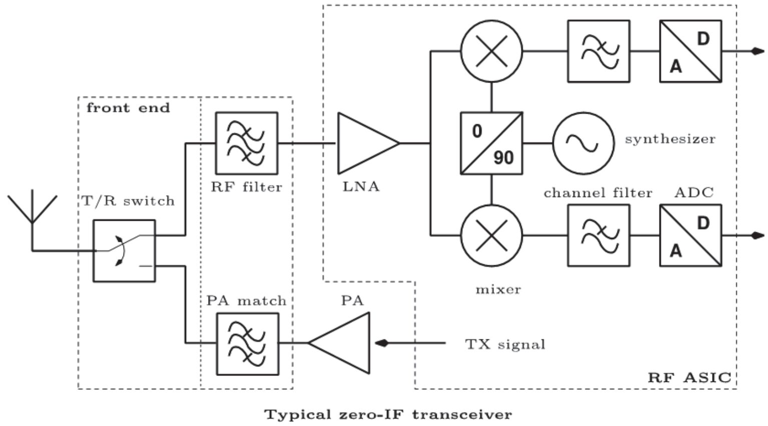


Figure 13 Typical zero-IF transceiver schematic

Noise figure model

A simplified receiver model can be derived by lumping the FE, RX and ADC into three cascaded blocks. This model cannot replace a rigorous analysis but will show the main parameter inter dependencies.

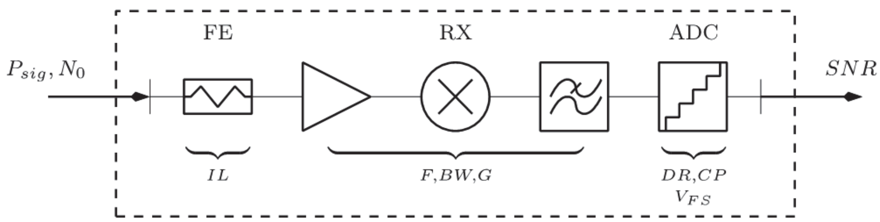


Figure 14 A simplified receiver model

Focusing on the small signal co-channel noise floor we can study the impact of various signal and linearity impairments to arrive at simple noise factor, or noise figure, expression.

Noise factor and noise floor

Assuming matched conditions we can use Friis' formula to find the noise factor at the receiver input as (linear units unless noted),

$F_{RX} = 1+(F_{LNA}-1)+(F_{ADC}-1)/G$.

The RX input referred small-signal co-channel noise floor will then equal

$N_{RX} = F_{LNA} \cdot N_0 + N_{ADC}/G$,

, where $N_0 = k \cdot T \cdot BW$ and N_{ADC} are the available noise power and the ADC effective noise floor in the channel bandwidth, respectively (k and T being Boltzmann's constant and absolute temperature, respectively). The ADC noise floor is typically set by a combination of quantization, thermal and intermodulation noise, but here we just assume a flat noise floor as defined by the ADC effective number of bits ($SINAD = 3/2 \cdot 2^{2 \cdot ENOB}$).

The effective gain from LNA input to ADC input, (G) depends on small-signal gain, AGC setting, selectivity and desensitization (saturation), but here we assume the gain is set such that the antenna referred input compression point (CP_i) corresponds to the ADC clipping level, i.e. the ADC full scale input voltage (V_{FS}).

For weak nonlinearities, there is a direct mathematical relation between CP and the third-order intercept point (IP_3) such that $IP_3 \approx CP + 10$ dB. For higher-order nonlinearities, the difference can be larger than 10 dB, but then CP is still a good estimate of the maximum signal level while inter-modulation for lower signal levels may be overestimated.

Compression point and gain

Between the antenna and the RX we have the FE with its associated insertion loss (IL>1), e.g. due to a T/R switch, a possible RF filter, and PCB/substrate losses. These losses have to be accounted for in the gain and noise expressions. Knowing IL, we can now find the CP_i that corresponds to the ADC clipping as

$CP_i = IL \cdot N_{ADC} \cdot DR_{ADC}/G$.

The antenna referred noise factor and noise figure will then become

$F_i = IL \cdot F_{RX} = IL \cdot F_{LNA} + CP_i/(N_0 \cdot DR_{ADC})$, and, $NF_i = 10 \cdot \log_{10}(F_i)$, respectively.

When comparing two designs, e.g. at 2 and ~30 GHz, respectively, the ~30 GHz IL will be significantly higher than that of the 2GHz. From the F_i expression we see that to maintain the same noise figure (NF_i) for the two carrier frequencies, we need to compensate the higher FE loss at ~30 GHz by improving the RX noise factor. This can be accomplished (i) by using a better LNA (ii) by relaxing the input compression point, i.e. increasing G, or (iii) by increasing the DR_{ADC}. Usually a good LNA is already used at 2GHz to achieve a low NF_i so this option is rarely possible. Relaxing CP_i is an option but this will reduce IP_3 and linearity performance will degrade. Finally, increasing DR_{ADC} comes at a power consumption penalty (4× per extra bit). Especially wideband ADCs may have a high power consumption, i.e. when BW is below some 100 MHz the $N_0 \cdot DR_{ADC}$ product (i.e. $BW \cdot DR_{ADC}$) is proportional to the ADC power consumption, but for higher bandwidths the ADC power consumption is proportional to $BW^2 \cdot DR_{ADC}$, penalizing higher BW, see the ADC section. Increasing DR_{ADC} is typically not an attractive option and it is inevitable that the ~30 GHz receiver will have a significantly higher NF_i than that of the 2GHz receiver.

Power spectral density and dynamic range

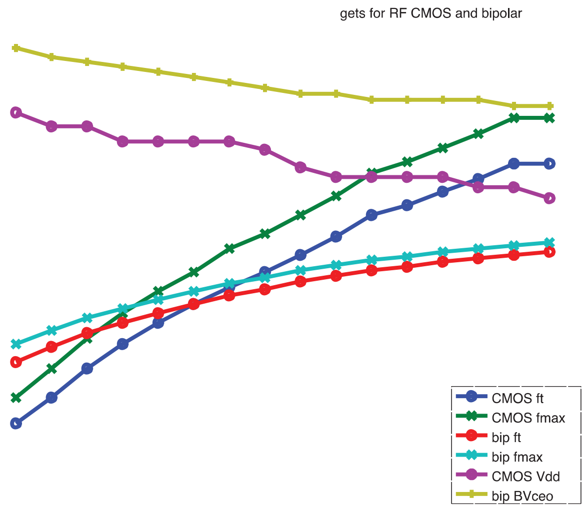
A signal consisting of many similar sub carriers will have a constant power-spectral density (PSD) over its bandwidth and the total signal power can then be found as $P = PSD \cdot BW$.

When signals of different bandwidths but similar power levels are received simultaneously, their PSDs will be inversely proportional to their BW. The antenna-referred noise floor will be proportional to BW and F_i, or $N_i = F_i \cdot k \cdot T \cdot BW$, as derived above. Since CP_i will be fixed, given by G and ADC clipping, the dynamic range, or maximum SNR, will decrease with signal bandwidth, i.e $SNR_{max} \propto 1/BW$.

The above signal can be considered as additive white Gaussian noise (AWGN) with an antenna-referred mean power level (P_{sig}) and a standard deviation (σ). Based on this assumption the peak-to-average-power ratio can be approximated as $PAPR = 20 \cdot \log_{10}(k)$, where the peak signal power is defined as $P_{sig} + k \cdot \sigma$, i.e. there are k standard deviations between the mean power level and the clipping level. For OFDM an unclipped PAPR of 10dB is often assumed (i.e. 3σ) and this margin must be subtracted from CP_i to avoid clipping of the received signal. An OFDM signal with an average power level, e.g., 3σ below the clipping level will result in less than 0.2 % clipping.

Carrier frequency and mm-wave technology aspects

Designing a receiver at, e.g., ~30 GHz with a 1 GHz signal bandwidth leaves much less design margin than what would be the case for a 2 GHz carrier with e.g. 50 MHz signal bandwidth as the IC technology speed is similar in both cases but the design margin and performance depends on the technology being much faster than the required signal processing.



The graph shows ITRS's expected evolution of some transistor parameters important for mm-wave IC design. Here f_t, f_{max}, and V_{dd} /Bvceo data from the ITRS 2007 targets for CMOS and bipolar RF technologies are plotted vs. the calendar year when the technology is anticipated to become available. For example, an RF CMOS device is expected to have a maximum V_{dd} of 800mV by 2016.

The free space wavelength at ~30 GHz is only 1 cm which is one tenth of what we are used to from existing 3GPP bands below 6 GHz. Antenna size and path loss are related to wavelength and carrier frequency, and to compensate the small physical size of a single antenna element we will have to use multiple antennas, e.g. array antennas. Then, when beam forming is used the spacing between antenna elements will still be related to the wavelength constraining the size of the FE and RX. Some of the implications of these frequency and size constraints are:

- The ratios $f_t/f_{carrier}$ and $f_{max}/f_{carrier}$, where f_t is the transistor transit frequency (i.e. when the RF device´s current gain is 0 dB), and where f_{max} is the maximum frequency of oscillation (i.e. when the extrapolated power gain is 0 dB), will be much lower at millimeter wave frequencies than for below 6 GHz applications. As receiver gain drops with operating frequency when this ratio is less than some 10 − 100×, the available gain at millimeter waves will be lower and consequently the device noise factor F_i higher (similar as if Friis' formula was applied to a transistor's internal noise sources).
- The breakdown voltage of active devices is inversely proportional to the maximum speed of the device due to the Johnson limit. I.e. $v_{sat} \cdot E_{br}$ = const. or $f_{max} \cdot V_{dd}$ = const. As a consequence the supply voltage will be lower for millimeter-wave devices compared to low

GHz ones. This will limit the CP_i and the maximum available dynamic range.

- Higher level of transceiver integration is required to save space, either as System-On-Chip or System-In-Package. This will limit the number of technologies suitable for the RF transceiver and limit F_{RX} .
- RF filters will have to be placed close to the antenna elements and fit into the array antenna. Consequently they have to be small, resulting in higher physical tolerance requirements, possibly at the cost of insertion loss and stop-band attenuation. That is, IL and selectivity gets worse. The filtering aspect for mm-wave frequencies is further elaborated in section 2.4.

Increasing the carrier frequency, $f_{carrier}$ from, say 2 GHz to ~30 GHz (i.e. >10×) has a significant impact on the circuit design and its RF performance. For example, modern high-speed CMOS devices are velocity saturated and their maximum operating frequency is inversely proportional to the minimum channel length, or feature size. This dimension halves roughly every four years, as per Moore's law (stating that complexity, i.e. transistor density, doubles every other year). With smaller feature sizes internal voltages must also be lowered to limit electrical fields to safe levels. Thus, designing a 30 GHz RF receiver corresponds to designing a 2 GHz receiver using about 15 years old low-voltage technology (i.e. today's breakdown voltage but 15 years old f_t, see figure based on ITRS device targets). With such a mismatch in device performance and design margin it is not to be expected to maintain 2GHz performance and power consumption at 30 GHz.

The signal bandwidth at mm-wave frequencies will also be significantly higher than at, say, 2GHz. For an active device, or circuit, the signal swing is limited by the supply voltage at one end and by thermal noise at the other. The available thermal noise power of a device is proportional to BW/g_m, where g_m is the intrinsic device gain (trans-conductance). As g_m is proportional to bias current we can see that the dynamic range then becomes the ratio

$$DR \propto V_{dd}^2 \cdot I_{bias}/BW = V_{dd} \cdot P/BW,$$

or

$$P \propto BW \cdot DR/ V_{dd}$$

Where P is the power dissipation.

Receivers for mm-wave frequencies will have increased power consumption due to higher BW, aggravated by the low-voltage technology needed for speed, compared to typical 2GHz receivers.

Thus, considering the thermal challenges given the significantly reduced area/volume for mm-wave products, the complex interrelation between linearity, NF, bandwidth and dynamic range in the light of power dissipation should be considered. We will further elaborate on this in the coming meetings.

3 Conclusion

In this paper, the discussion on some important and fundamental aspects related to mm-wave technologies is initiated with the intention to reach a common understanding over what mm-wave technologies can offer and how requirements can be appropriately derived. As RAN4 work has been limited to frequency bands below 6 GHz, alignment of understanding of the technology characteristics is a quite important step before the more detailed requirement work is started. In addition as we have very stringent time plan for ITU-R-response, this paper give an insight from technology point of view which needs to be considered in addition to other co-existence studies for 24-86 GHz.

The need for high integrated mm-wave systems with many transceivers and antennas would require careful and often complex consideration regarding the power efficiency and heat dissipation in small area/volume affecting the achievable performance.

Areas such as DA/AD converters, power amplifiers and the achievable power versus efficiency as well as linearity are further discussed. In addition, we provide some detailed insight into the receiver essential metrics such as noise figure, bandwidth, dynamic range, power dissipation and the complex dependencies. The mechanism for frequency generation as well as phase noise aspects is also covered in this paper. The filters for mm-waves is another important part of this paper indicating the achievable performance for various technologies and the feasibility of integrating such filters into NR implementations.

This is in the light of the need for highly integrated mm-wave systems with many transceivers and antennas which would require careful and often complex consideration regarding the power efficiency and heat dissipation in small area/volume influenced by aspects described in this paper.

We will further elaborate in the areas covered in this paper and contribute on additional areas in the coming meetings where more time units are available for NR and encourage other companies to contribute in this area.

4 References

[1] R4-164167, "Additional aspects for NR BS core requirements", Ericsson